

Taos Schematics Skylake/Kabylake -U

2016-12-23

REV : A00



DY : None Installed

UMA: UMA only installed

OPS: DISCRTE OPTIMUS installed

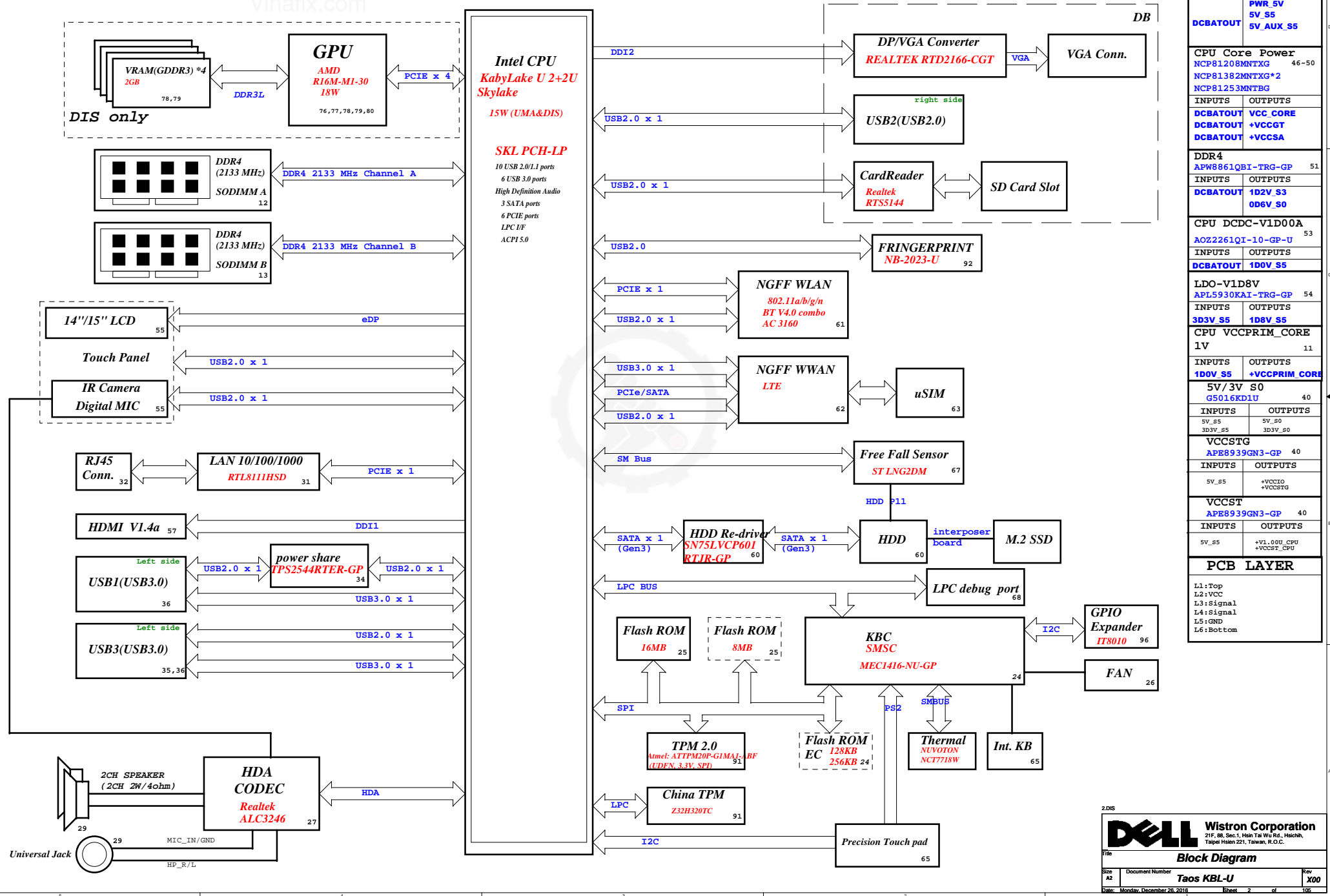
2.DIS

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Title			
Cover Page			
Size A3	Document Number Taos KBL-U		Rev X00
Date: Monday, December 26, 2016		Sheet 1	of 105

Project code:
Taos14 -->4PD09Z010001
Taos15 -->4PD0A1010001
PCB P/N: 16852
Revision: A00

Taos KBL-U/SKL-U Block Diagram

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2.0IS


Main Func = CPU

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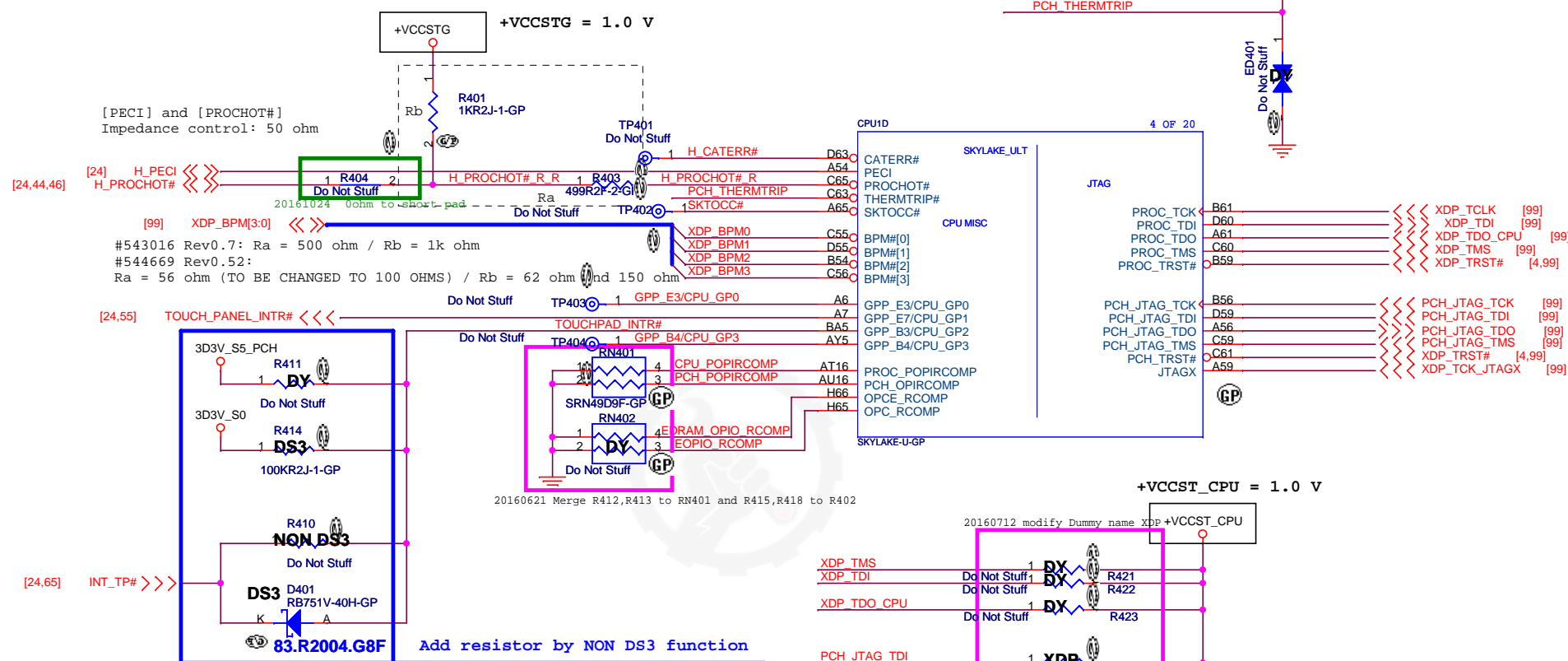


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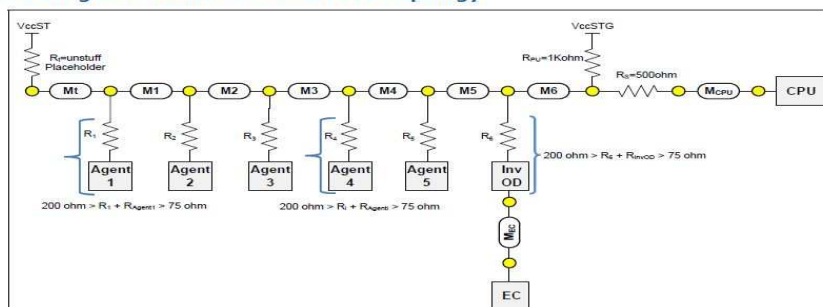
Main Func = CPU

#544669 CRB Rev0.52

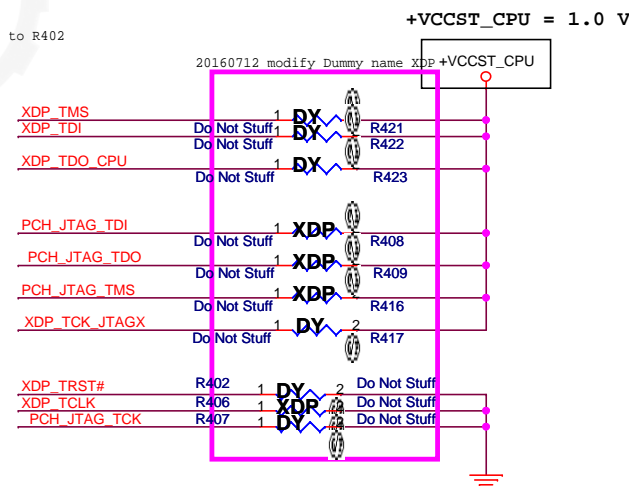


(#543016) PROCHOT# Routing Guidelines

Figure 10-1. Routing Illustration for PROCHOT# Topology



Main route (M1+M2+M3+M4+M5+M6+MCPU): 1-12 inches



2.DIS

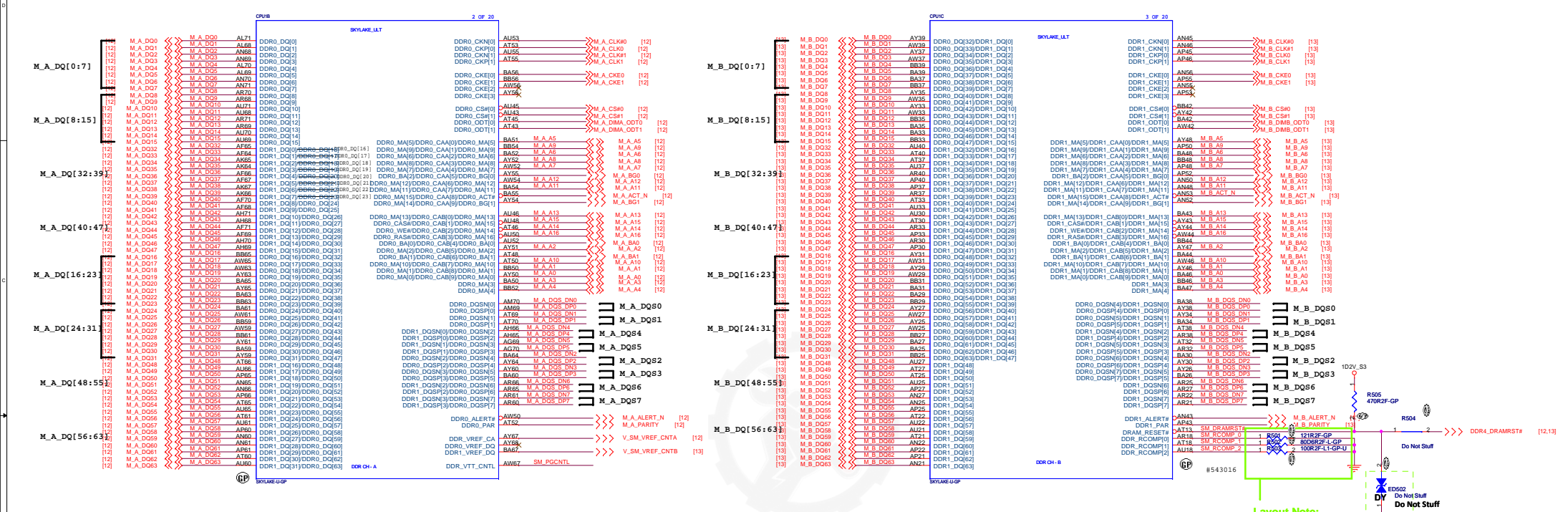


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Title	CPU_ (JTAG/CPU SIDE BAND)
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Size	Document Number	Rev
Custom	Taos KBI-II	X00

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DQ Bit Swapping is allowed within the same byte, and Byte Swapping is allowed within the same channel.
Clock (CLK and CLK#) and Strobe (DQS and DQS#) differential signal swapping within a pair is not allowed. Also differential clock pair to clock pair swapping within a channel is not allowed.

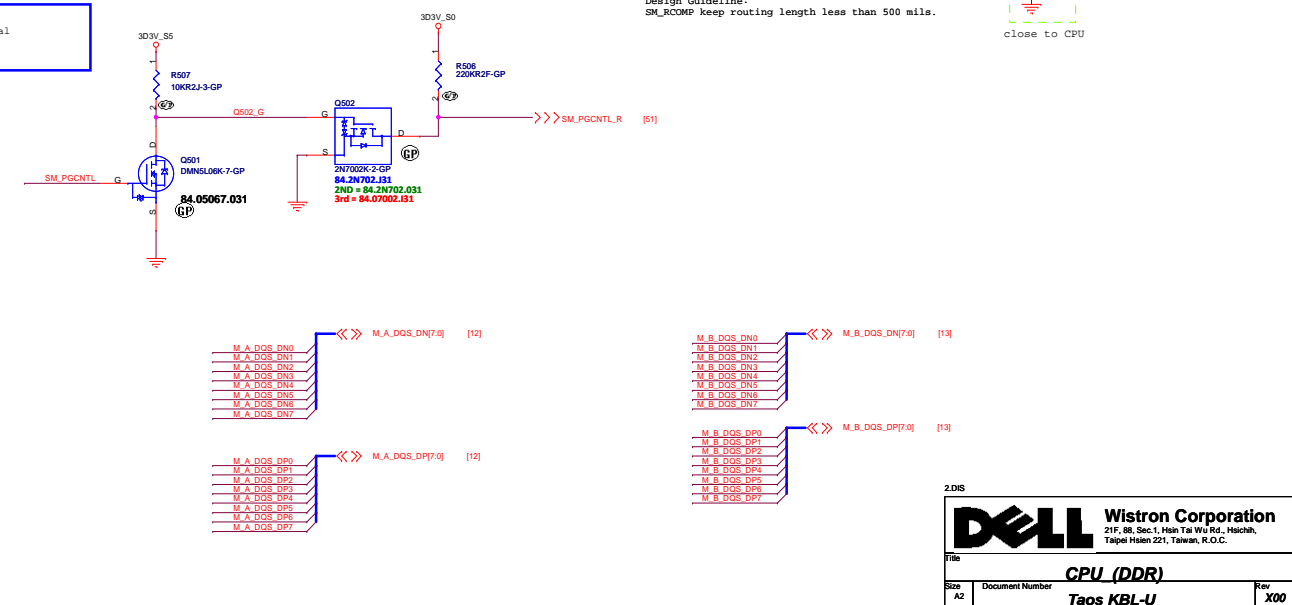
PDG: DDR/ODT

4.17 SKL U and SKL Y System Memory ODT Signal Connectivity Details

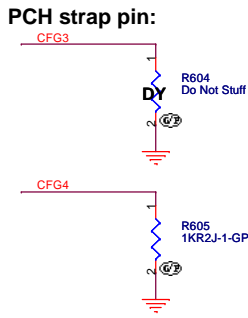
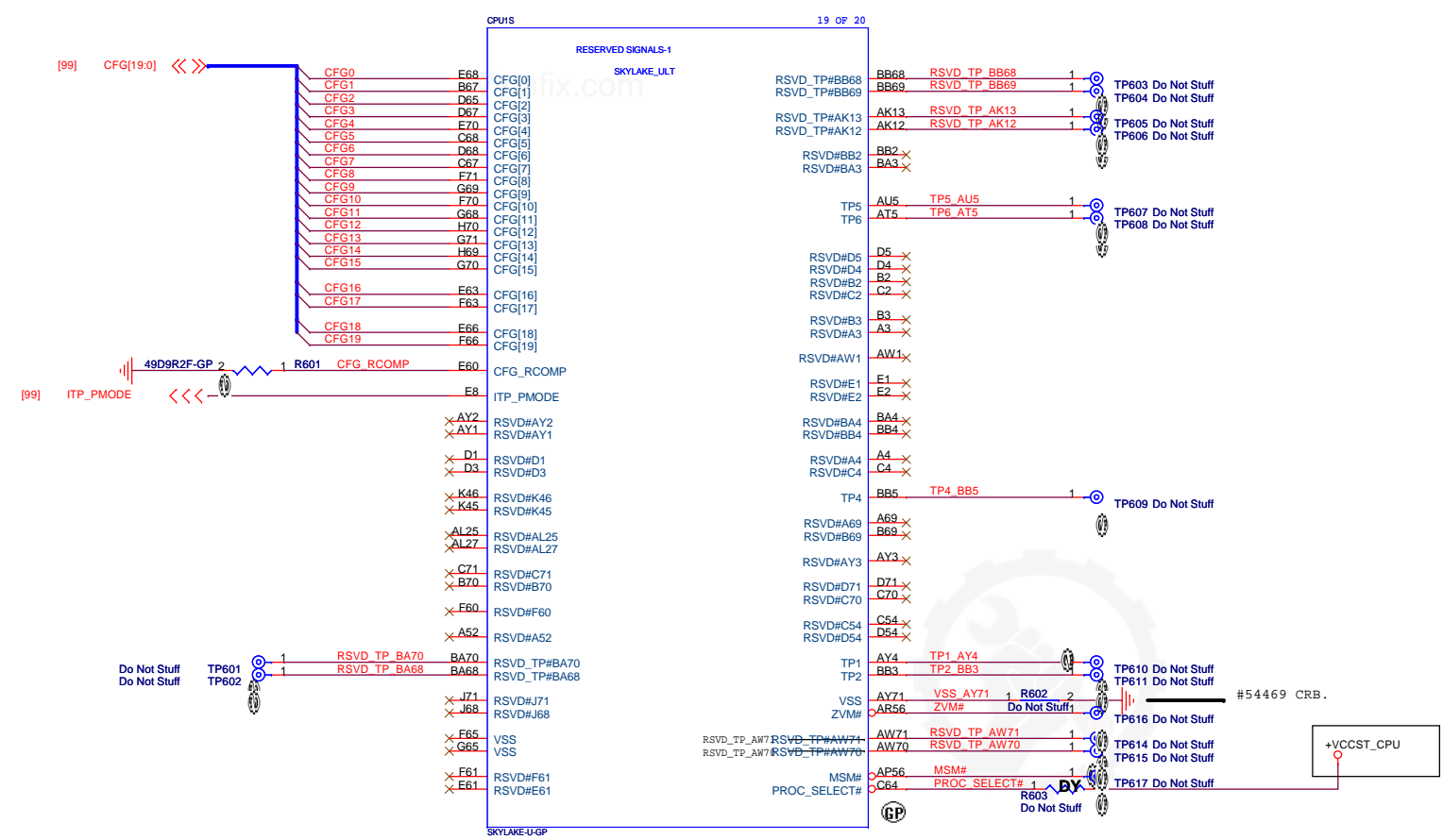
Processor	Memory Type	Side	Signal	Rule	Notes
SKL-Y	LPDDR3 Memory Down	Processors	DDR0_ODT[0]	Processor's ODT[0] connected to DRAM's ODT. T-topology connection	1,2
			DDR1_ODT[0]	Processor's ODT[1] connected to DRAM's ODT. T-topology connection	1,2
SKL-U	LPDDR3 Memory Down	Processors	DDR0_ODT[1:0]	Processor's ODT[0] connected to DRAM's ODT. T-topology connection.	1,2
			DDR1_ODT[1:0]	Processor's ODT[1] connected to DRAM's ODT. T-topology connection.	1,2
DDR3L Memory Down	Processor	Processors	DDR0_ODT[1:0]	Processor's ODT[0] connected to DRAM's Rank0 ODT.	3,4
			DDR1_ODT[1:0]	Processor's ODT[1] connected to DRAM's Rank1 ODT.	3,4
DDR3L SO-DIMM	Processor	Processors	DDR0_ODT[1:0]	Processor's ODT[0] connected to DIMM's Rank0 ODT.	1,3
			DDR1_ODT[1:0]	Processor's ODT[1] connected to DIMM's Rank1 ODT.	1,3
DDR3L Mixed Memory Down	Processor	Processors	DDR0_ODT[1:0]	Processor's ODT[0] connected to DIMM's Rank0 ODT. Processor's ODT[1] connected to DRAM's Rank0 ODT.	3,4
			DDR1_ODT[1:0]	Processor's ODT[1] connected to DIMM's Rank1 ODT. Processor's ODT[0] connected to DRAM's Rank1 ODT.	3,4
DDR4 Memory Down	Processor	Processors	DDR0_ODT[1:0]	Processor's ODT[0] connected to DRAM's Rank0 ODT. Processor's ODT[1] connected to DRAM's Rank1 ODT.	3,4
			DDR1_ODT[1:0]	Processor's ODT[1] connected to DRAM's Rank0 ODT. Processor's ODT[0] connected to DRAM's Rank1 ODT.	3,4
DDR4 SO-DIMM	Processor	Processors	DDR0_ODT[1:0]	Processor's ODT[0] connected to DIMM's Rank0 ODT.	1,3
			DDR1_ODT[1:0]	Processor's ODT[1] connected to DIMM's Rank1 ODT.	1,3

Notes:

- For additional ODT signal connection details, reference the Customer Reference Board (CRB) schematics and board files (BUP2 - SKL-U (DDR3), BUP3 - SKL-U (DDR3), BUP4 - SKL-U (DDR3), BUP5 - SKL-U (DDR3), BUP6 - SKL-U (DDR3), BUP7 - SKL-U (DDR3), BUP8 - SKL-U (DDR3), BUP9 - SKL-U (DDR3), BUP10 - SKL-U (DDR3), BUP11 - SKL-U (DDR3), BUP12 - SKL-U (DDR3), BUP13 - SKL-U (DDR3), BUP14 - SKL-U (DDR3), BUP15 - SKL-U (DDR3), BUP16 - SKL-U (DDR3), BUP17 - SKL-U (DDR3), BUP18 - SKL-U (DDR3), BUP19 - SKL-U (DDR3), BUP20 - SKL-U (DDR3), BUP21 - SKL-U (DDR3), BUP22 - SKL-U (DDR3), BUP23 - SKL-U (DDR3), BUP24 - SKL-U (DDR3), BUP25 - SKL-U (DDR3), BUP26 - SKL-U (DDR3), BUP27 - SKL-U (DDR3), BUP28 - SKL-U (DDR3), BUP29 - SKL-U (DDR3), BUP30 - SKL-U (DDR3), BUP31 - SKL-U (DDR3), BUP32 - SKL-U (DDR3), BUP33 - SKL-U (DDR3), BUP34 - SKL-U (DDR3), BUP35 - SKL-U (DDR3), BUP36 - SKL-U (DDR3), BUP37 - SKL-U (DDR3), BUP38 - SKL-U (DDR3), BUP39 - SKL-U (DDR3), BUP40 - SKL-U (DDR3), BUP41 - SKL-U (DDR3), BUP42 - SKL-U (DDR3), BUP43 - SKL-U (DDR3), BUP44 - SKL-U (DDR3), BUP45 - SKL-U (DDR3), BUP46 - SKL-U (DDR3), BUP47 - SKL-U (DDR3), BUP48 - SKL-U (DDR3), BUP49 - SKL-U (DDR3), BUP50 - SKL-U (DDR3), BUP51 - SKL-U (DDR3), BUP52 - SKL-U (DDR3), BUP53 - SKL-U (DDR3), BUP54 - SKL-U (DDR3), BUP55 - SKL-U (DDR3), BUP56 - SKL-U (DDR3), BUP57 - SKL-U (DDR3), BUP58 - SKL-U (DDR3), BUP59 - SKL-U (DDR3), BUP60 - SKL-U (DDR3), BUP61 - SKL-U (DDR3), BUP62 - SKL-U (DDR3), BUP63 - SKL-U (DDR3), BUP64 - SKL-U (DDR3), BUP65 - SKL-U (DDR3), BUP66 - SKL-U (DDR3), BUP67 - SKL-U (DDR3), BUP68 - SKL-U (DDR3), BUP69 - SKL-U (DDR3), BUP70 - SKL-U (DDR3), BUP71 - SKL-U (DDR3), BUP72 - SKL-U (DDR3), BUP73 - SKL-U (DDR3), BUP74 - SKL-U (DDR3), BUP75 - SKL-U (DDR3), BUP76 - SKL-U (DDR3), BUP77 - SKL-U (DDR3), BUP78 - SKL-U (DDR3), BUP79 - SKL-U (DDR3), BUP80 - SKL-U (DDR3), BUP81 - SKL-U (DDR3), BUP82 - SKL-U (DDR3), BUP83 - SKL-U (DDR3), BUP84 - SKL-U (DDR3), BUP85 - SKL-U (DDR3), BUP86 - SKL-U (DDR3), BUP87 - SKL-U (DDR3), BUP88 - SKL-U (DDR3), BUP89 - SKL-U (DDR3), BUP90 - SKL-U (DDR3), BUP91 - SKL-U (DDR3), BUP92 - SKL-U (DDR3), BUP93 - SKL-U (DDR3), BUP94 - SKL-U (DDR3), BUP95 - SKL-U (DDR3), BUP96 - SKL-U (DDR3), BUP97 - SKL-U (DDR3), BUP98 - SKL-U (DDR3), BUP99 - SKL-U (DDR3), BUP100 - SKL-U (DDR3).
- DDR3L ODT input is held high (active). N/A N/A is defined by R105 as high-Z in both ranks, when a Rank receives write command R enables R/W via (set by R105 after power loading). Otherwise ODT sets R/W N/A (high-Z).
- These guidelines are related to DDR3L supported Memory down topologies only. 2R x16 DCP single side, 2R x16 DCP dual side and 2R x16 DCP dual side.



Main Func = CPU



[BDW Only]PHYSICAL_DEBUG_ENABLED (DFX PRIVACY)	
CFG[3]	0 : ENABLED SET DFX ENABLED BIT IN DEBUG INTERFACE MSR
	1 : DISABLED

DISPLAY PORT PRESENCE STRAP	
CFG[4]	0 : ENABLED An external Display Port device is connected to the Embedded Display Port.
	1 : DISABLED (Default) No Physical Display Port attached to Embedded DisplayPort*. No connect for disable.

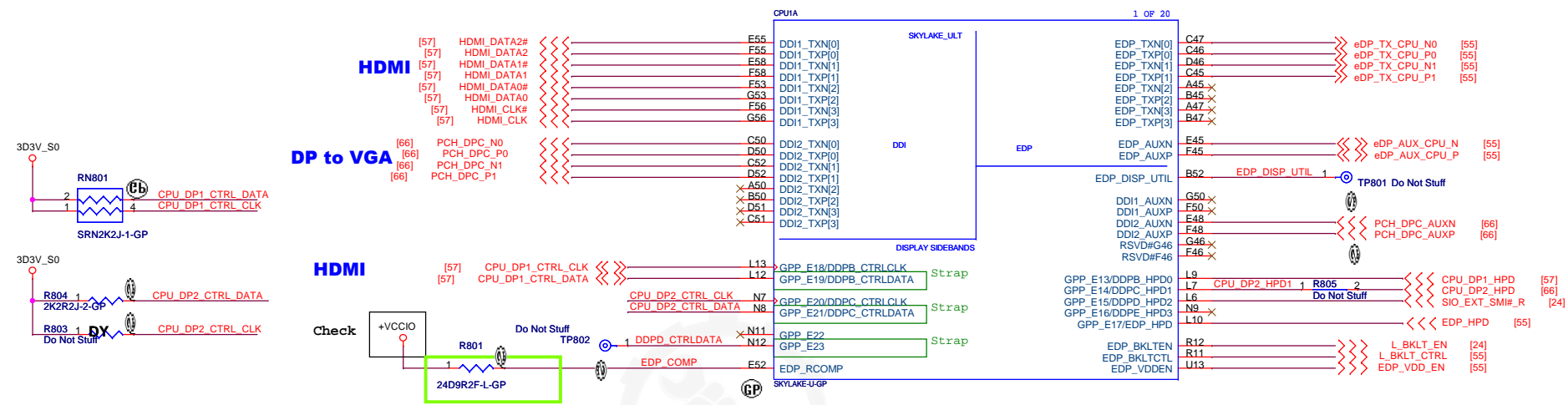
CFG TERMINATIONS

20140807 david

#544669 Rev0.52 (CRB)

SKL(#543016):
Processor strap CFG[4] should be pulled low to enable embedded DisplayPort*

Vinafix.com



(#543016) eDP_RCOMP Guideline

Signal	Trace Width	Isolation Spacing	Resistor Value	Length
eDP_RCOMP	20 mils	25 mils	24.9 Ω \pm 1%	Max = 100 mils

(#543016) The Skylake U/Y processor supports only two DDI ports - Port 1 and Port 2.

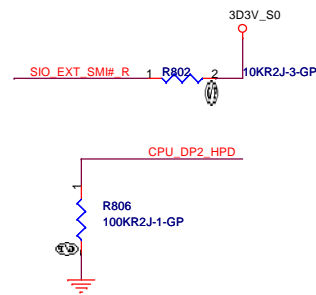
(#543016) DDI Disabling and Termination Guidelines

Port	Strap	Enable Port	Disable Port
Port 1	DDPB_CTRLDATA	PU to 3.3 V with 2.2-k \pm 5% resistor	NC
Port 2	DDPC_CTRLDATA	PU to 3.3 V with 2.2-k \pm 5% resistor	NC

Strap pin:

Port B / Port C Detected	Sampled at rising edge of PCH_PWROK
DDPB_CTRLDATA	0 = Port B is not detected. ★ 1 = Port B is detected.
DDPC_CTRLDATA	0 = Port C is not detected. ★ 1 = Port C is detected.

These two signals have weak internal pull-down.
Design Guideline:
Skylake processor signal eDP_RCOMP should be connected to the VCCIO rail via a single 24.9 \pm 1% Ω resistor.




Main Func = CPU

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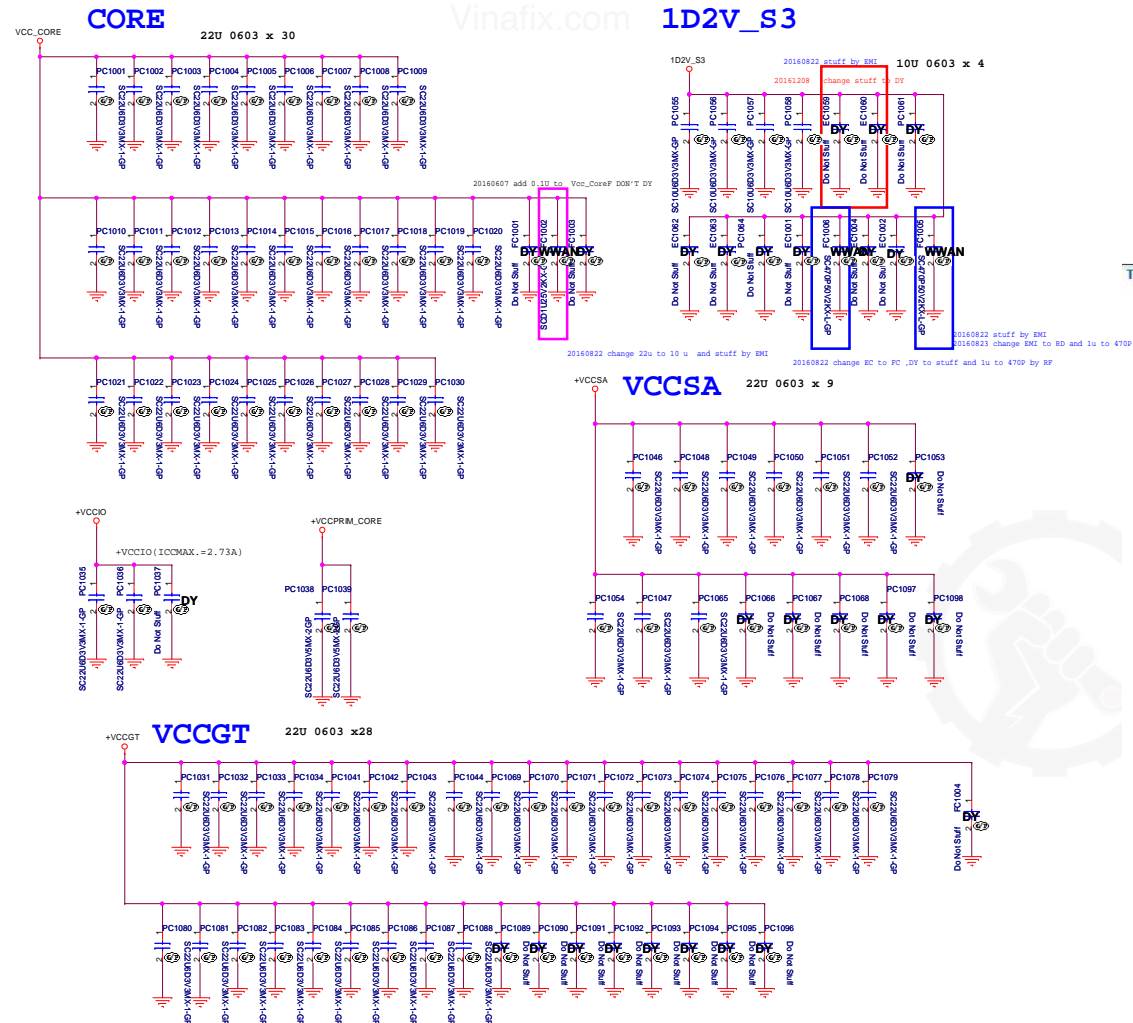


Table 53-3. SKL U Bulk Decoupling Requirements

Bulk Decoupling Locations	Requirements	Notes
VCC Power Plane at VR output	1x 220uF (Ø4.5m0 ESR)	Placed at primary side near to VR output
	1x 220uF (Ø4.5m0 ESR)	Placed at backside side near to VR output
VCCGT Power Plane at VR output	2x 220uF (Ø4.5m0 ESR)	Placed at primary side near to VR output
	1x 220uF (Ø4.5m0 ESR)	Placed at primary side near to VR output Additional components needed when supporting 23e
VCCGTx Power Plane at VR output	1x 220uF (Ø4.5m0 ESR)	Placed at primary side near to VR output Only needed when supporting 23e
VCCIO Power Plane at VR output	2x 47uF 0805	Placed at primary side near to VR output
VCCSA Power Plane at VR output	2x 47uF 0805	Placed at primary side near to VR output

Note: These requirements are based on 1MHz switching frequency VR with bandwidth of up to 250kHz.

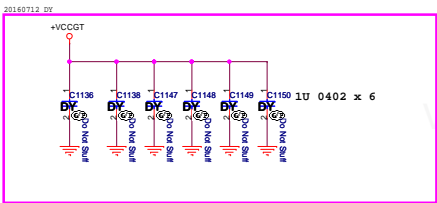
Table 53-4. Decoupling Requirements for SKL U Processor (Sheet 1 of 2)

Domain	Backside cap	Primary side cap	Placement guideline
VCC	9x 22uF 0603		Place on secondary side, underneath the package
	7x 10uF 0402		
	15x 1uF 0201		
		8x 47uF 0805 (6.3V)	
VCCGT		8x 10uF 0402	Place on secondary side, underneath the package
	10x 10uF 0402		
	12x 1uF 0201		
		3x 47uF 0805 (6.3V) ¹	
VCCGTx		7x 22uF 0603	Place as close to the package as possible
		3x 47uF 0805	
		5x 22uF 0603	
VCCSA			Place on secondary side, underneath the package
	7x 10uF 0402		
	7x 1uF 0201		
		6x 10uF 0402	
VCCIO			Place on secondary side, underneath the package
	2x 10uF 0402		
	4x 1uF 0201		
		4x 1uF 0402	
VDDQ			Place on secondary side, underneath the package
	2x 10uF 0402		
	4x 1uF 0201		
		4x 10uF 0402	
VDDQC	1x 1uF 0201		Place on secondary side, underneath the package
VCCPLL		1x 1uF 0402	Place as close to the package as possible
VCCST		1x 1uF 0402	Place as close to the package as possible

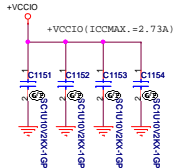
Table 53-4. Decoupling Requirements for SKL U Processor (Sheet 2 of 2)

Domain	Backside cap	Primary side cap	Placement guideline
VCCSTG	1x 1uF 0402		Place on secondary side, underneath the package Placeholder only
VCCEPIO	2x 10uF 0402		Place on secondary side, underneath the package
VCCOPC	1x 10uF 0402 6x 1uF 0201		Place on secondary side, underneath the package

Main Func = CPU



VCCIO



PCH DERIVED RAILS

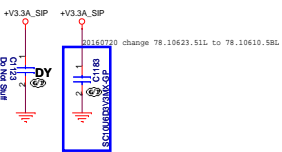
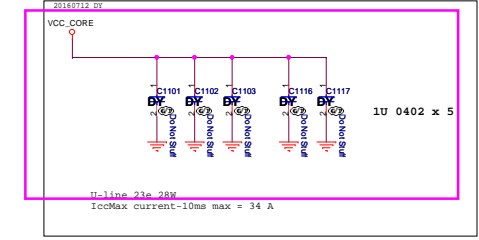
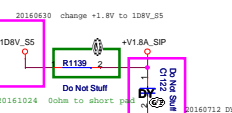
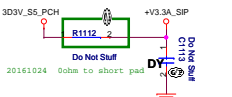
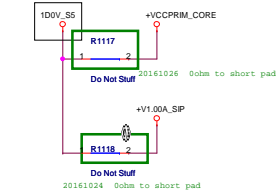


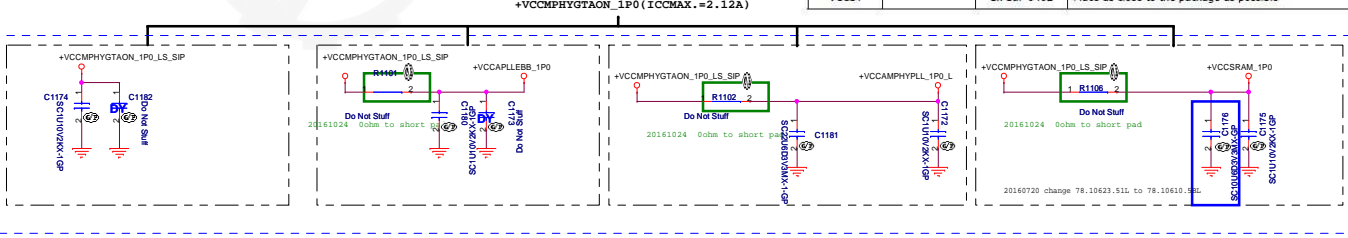
Table 53-3. SKL U Bulk Decoupling Requirements

Bulk Decoupling Locations	Requirements	Notes
VCC Power Plane at VR output	1x 220uF (@4.5mΩ ESR) 1x 220uF (@4.5mΩ ESR)	Placed at primary side near to VR output Placed at backside near to VR output
VCCGT Power Plane at VR output	2x 220uF (@4.5mΩ ESR) 1x 220uF (@4.5mΩ ESR)	Placed at primary side near to VR output Additional components needed when supporting 23e
VCCGTx Power Plane at VR output	1x 220uF (@4.5mΩ ESR)	Placed at primary side near to VR output Only needed when supporting 23e
VCCIO Power Plane at VR output	2x 47uF 0805	Placed at primary side near to VR output
VCCSA Power Plane at VR output	2x 47uF 0805	Placed at primary side near to VR output

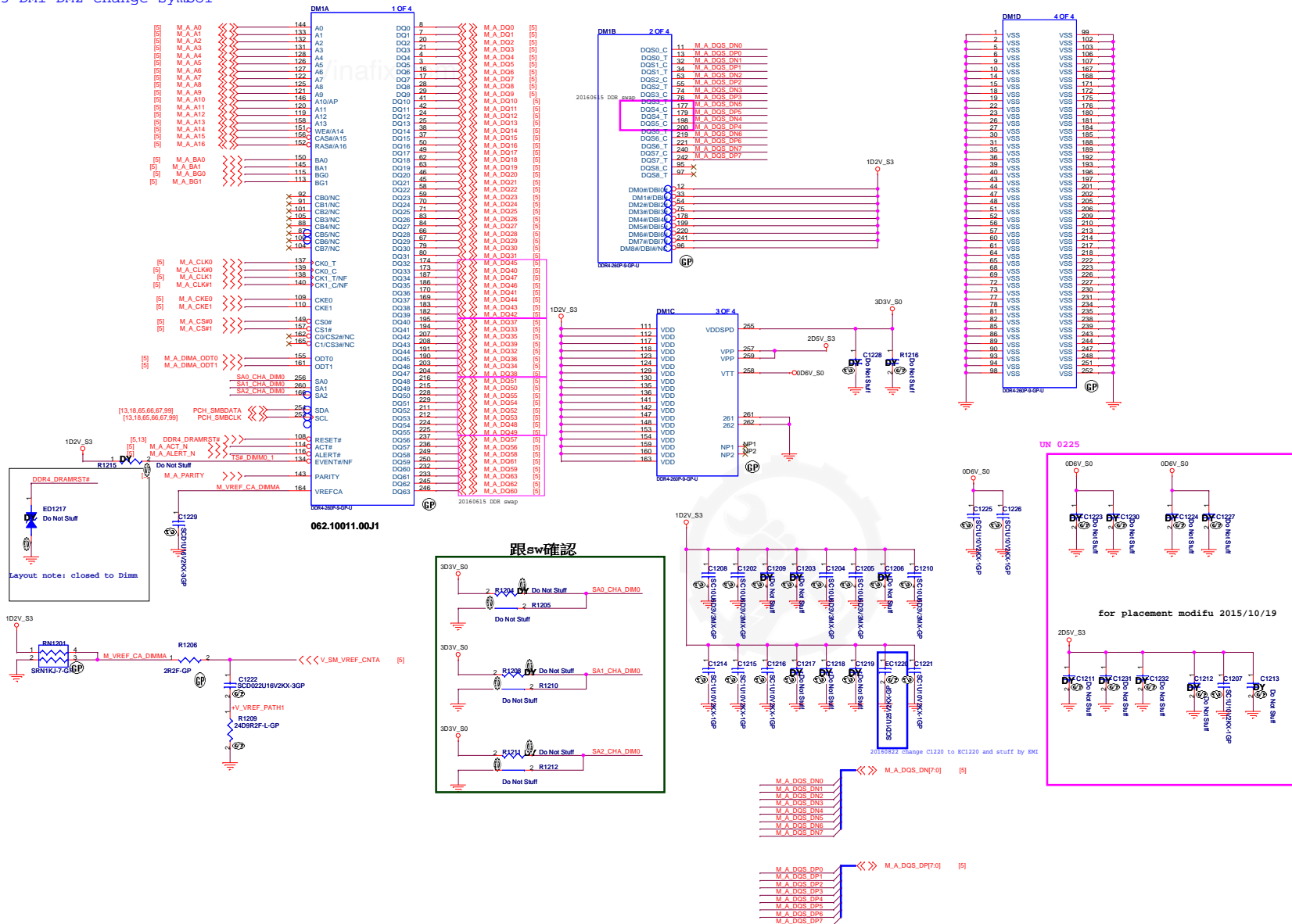
Note: These requirements are based on 1MHz switching frequency VR with bandwidth of up to 250kHz.

Table 53-4. Decoupling Requirements for SKL U Processor (Sheet 1 of 2)

Domain	Backside cap	Primary side cap	Placement guideline
VCC	9x 22uF 0603		Place on secondary side, underneath the package
	7x 10uF 0402		
	15x 1uF 0201		
		8x 47uF 0905 (6.3V) ¹	
VCCGT	10x 10uF 0402		Place on secondary side, underneath the package
	12x 1uF 0201		
		3x 47uF 0905 (6.3V) ¹	
		7x 22uF 0603	
VCCGTx	8x 10uF 0402		Place on secondary side, underneath the package Only needed when supporting 23e
		3x 47uF 0805	
		5x 22uF 0603	
		8x 22uF 0603	
VCCSA	7x 10uF 0402		Place on secondary side, underneath the package
	7x 1uF 0201		
VCCIO	2x 10uF 0402		Place on secondary side, underneath the package
	4x 1uF 0201		
VDDQ	2x 10uF 0402		Place on secondary side, underneath the package
	4x 1uF 0201		
VDDQC	1x 1uF 0201		Place on secondary side, underneath the package
		4x 10uF 0402	
VCCPLL	1x 1uF 0402		Place as close to the package as possible
VCCST	1x 1uF 0402		Place as close to the package as possible

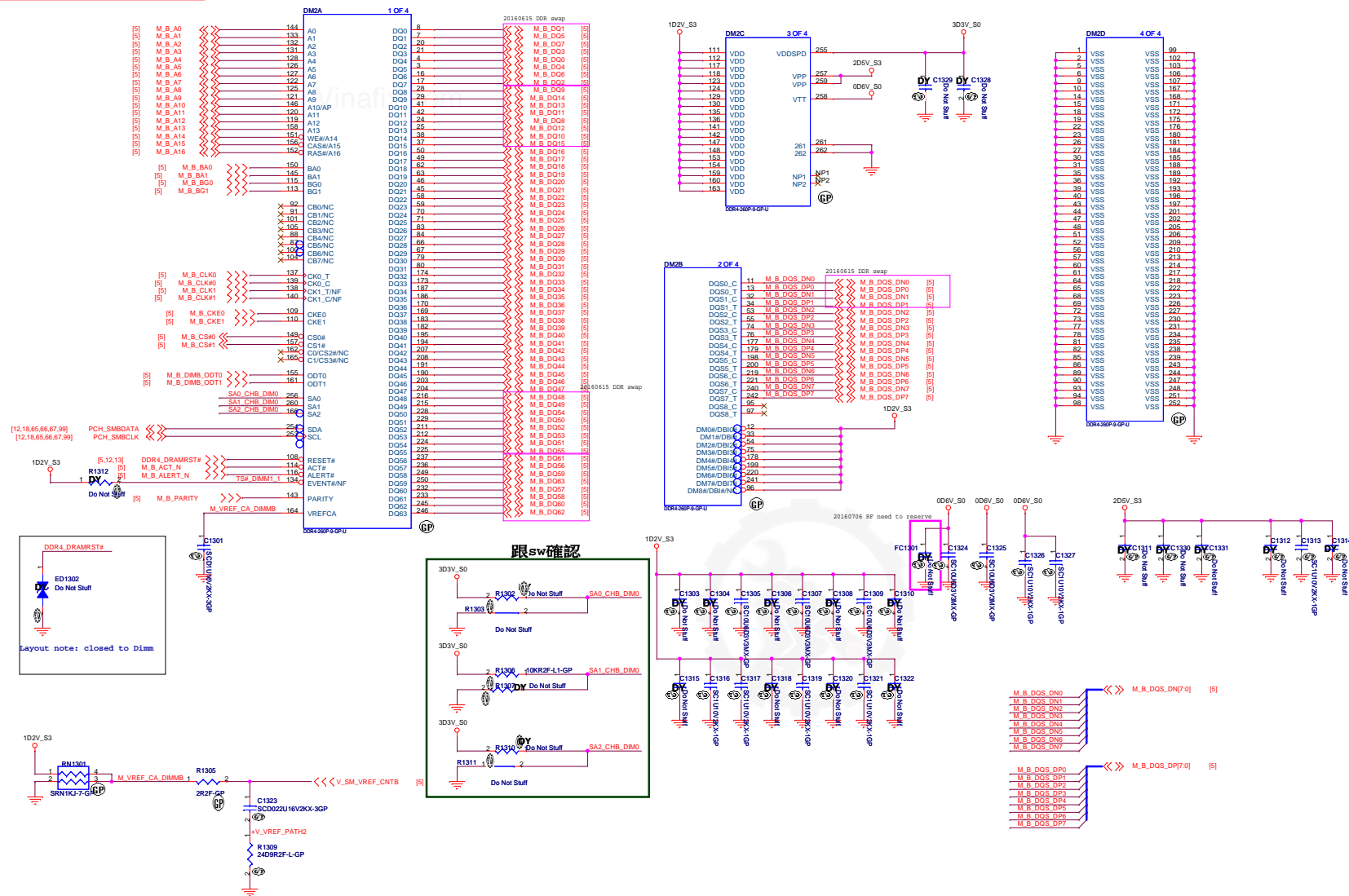


20160815 DM1 DM2 change symbol



2.DIS

Main Func = DDR4 SODIMM




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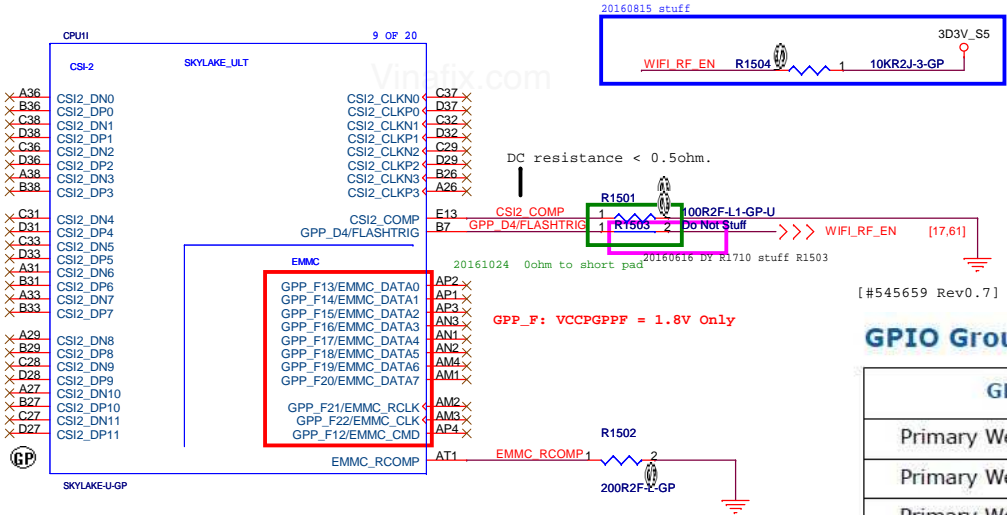
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Main Func = PCH

Table 8-1. Switchable Graphics GPIO Requirements

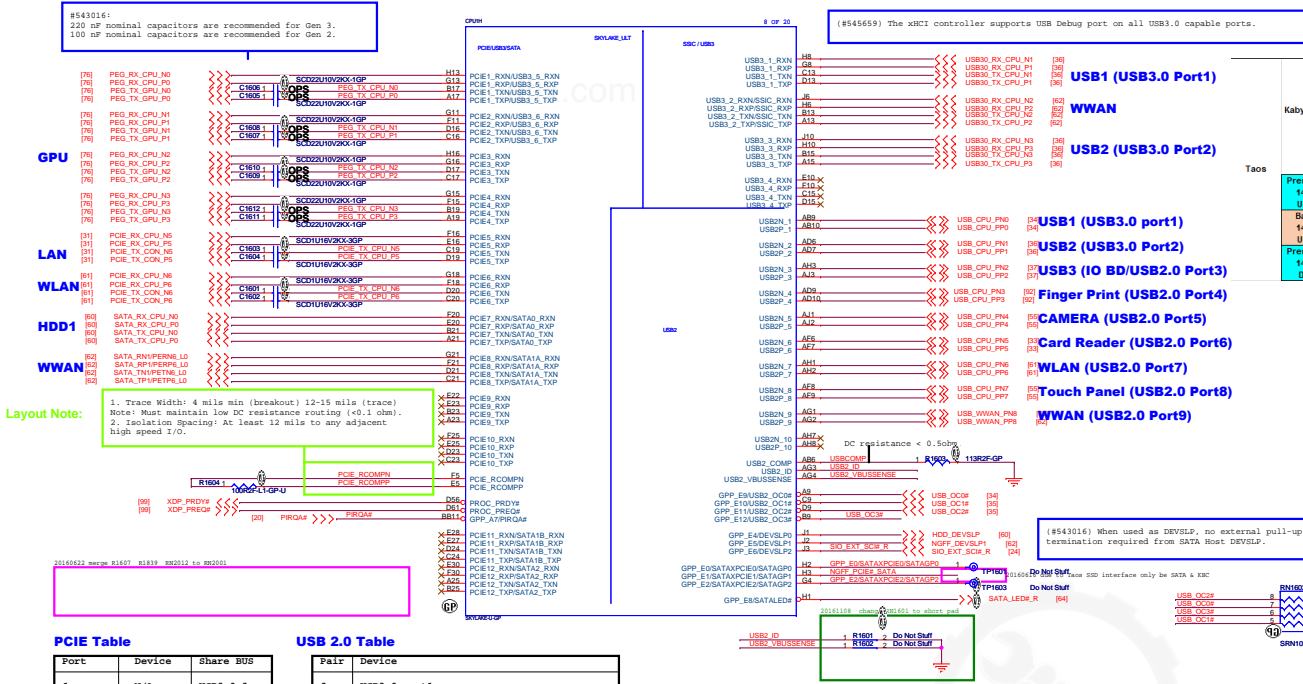
GPIO	Usage
DGPU_PWR_EN#	BIOS drives to turn on/off the discrete graphics power.
DGPU_PWROK	dGPU voltage regulator drives to indicate power status to the PCH. It enables clocks to dGPU.
DGPU_HOLD_RST#	Discrete Graphics Enable signal. BIOS controls and a PCH GPIO drives. It gates Platform Reset to enable Reset for the dGPU.
DGPU_PRSENT#	Used only by the CRB or if Graphic Cards requiring AC caps on the motherboard or add-in card is supported on the platform to indicate that a card is present.



GPIO Group Summary

GPIO Group	Power Pins	Voltage
Primary Well Group A (GPP_A)	VCCPGPPA	1.8V or 3.3V
Primary Well Group B (GPP_B)	VCCPGPPB	1.8V or 3.3V
Primary Well Group C (GPP_C)	VCCPGPPC	1.8V or 3.3V
Primary Well Group D (GPP_D)	VCCPGPPD	1.8V or 3.3V
Primary Well Group E (GPP_E)	VCCPGPPE	1.8V or 3.3V
Primary Well Group F (GPP_F)	VCCPGPPF	1.8V
Primary Well Group G (GPP_G)	VCCPGPPG	1.8V or 3.3V
Deep Sleep Well Group (GPD)	VCCPDSW_3p3	3.3V

Main Func = PCH



Layout Note:
1. Trace Width: 4 mils min (breakout) 12-15 mils (trace).
Note: Must maintain low DC resistance routing (<0.1 ohm).
2. Isolation Spacing: At least 12 mils to any adjacent high speed I/O.

PCIe Table

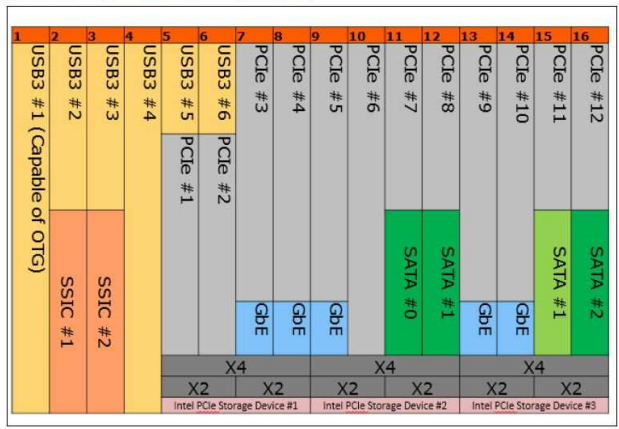
Port	Device	Share BUS
1	N/A	USB3_0_3
2	N/A	USB3_0_4
3	WLAN	
4	LAN	
5 (L0-L3)	GPU	
6 (L3)	HDD	SATA0
6 (L2)	N/A	
6 (L0-L2)	N/A	

USB 2.0 Table

Pair	Device
0	USB3.0 port1
1	USB3.0 Port2
2	USB2.0 Port3 (IOBD)
3	Finger print
4	CAMERA
5	Card Reader
6	Touch Panel
7	WLAN

#545659 (BKL_PCH_U_V_R00 Rev0.7)

Figure 3-1. HSIO Muxing on SKL PCH-LP (U Series)



update 0509

		1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16															
		USB3-2				PCe-1				PCe-2				PCe-3			
Taos	USB3-1 OTG	SSIC-1				X2				X2				X2			
	SSIC-1	X4				X2				X2				X2			
	SSIC-1	PCie Controller #1				PCie Controller #2 (Cycle Router 2)				PCie Controller #3 (Cycle Router 3)							
	SSIC-1	Discrete Graphics x4				LOM				LOM				LOM			
Premium 1415 UMA	Ext Port 1	M.2 3042 (LTE)	Ext Port 2							M.2 3030 (WLAN)	HDD SATA only 20pin Conn	M.2 3042 (SSD Cache)					
Basic 1415	Ext Port 1	M.2 3042 (LTE)	Ext Port 2							M.2 3030 (WLAN)	HDD SATA only 20pin Conn	M.2 3042 (SSD Cache)					
Premium 1415 BSC	Ext Port 1	M.2 3042 (LTE)	Ext Port 2							M.2 3030 (WLAN)	HDD SATA only 20pin Conn	M.2 3042 (SSD Cache)					

USB2.0 (10 ports)												
USB2-1 OTG	USB2-2	USB2-3	USB2-4	USB2-5	USB2-6	USB2-7	USB2-8	USB2-9	USB2-10	eDP	D0i-2 DP-VGA Conv	D0i-1
Ext Port 1	Ext Port 2	Ext Port 3 2.0 only	FPR	UF Camera	SD Reader	M.2 3030 (BT)	LCD Touch	M.2 3042 (WWAN)		LCD	VGA	HDMI
Ext Port 1	Ext Port 2	Ext Port 3 2.0 only	FPR	UF Camera	SD Reader	M.2 3030 (BT)	LCD Touch	M.2 3042 (WWAN)		LCD	VGA	HDMI
Ext Port 1	Ext Port 2	Ext Port 3 2.0 only	FPR	UF Camera	SD Reader	M.2 3030 (BT)	LCD Touch	M.2 3042 (WWAN)		LCD	VGA	HDMI

#543016 When used as DEVSUP, no external pull-up or pull-down termination required from SATA Host DEVSUP.

#543016 Unused SATA0[2:0]/GPP_E[2:0] pins must be terminated to either 3.3 V rail or GND using 8.2 kΩ to 10 kΩ on the motherboard. Do not use both pull-up and pull-down. Either pull-up or pull-down is acceptable.

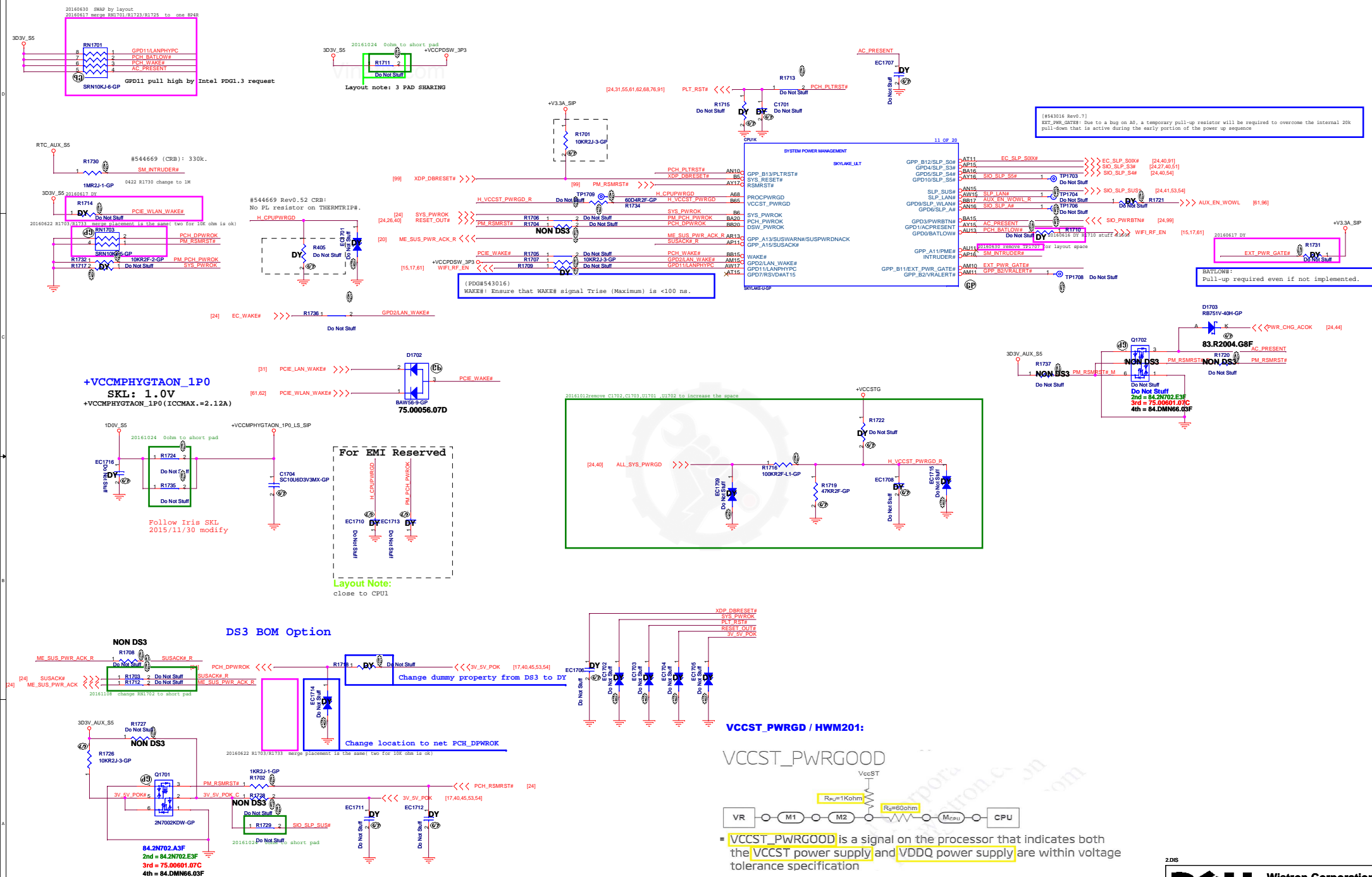
Table 24-2. PCI Express* Port Feature Details

SKL	Max Device (Ports)	Max Lanes	PCIe* Gen Type	Encoding	Transfer Rate (MT/s)	Theoretical Max Bandwidth (GB/s)		
						x1	x2	x4
U	6	12	1	8b/10b	2500	0.25	0.50	1.00
			2	8b/10b	5000	0.50	1.00	2.00
			3	128b/130b	8000	1.00	2.00	3.94
Y	5	10	1	8b/10b	2500	0.25	0.50	1.00
			2	8b/10b	5000	0.50	1.00	2.00

Table 24-3. PCI Express* Link Configurations Supported

SKL	PCIe Link Config	PCI Express* Lanes																	
		1	2	3	4	5	6	7	8	9	10	11	12						
U	1x4	Port1				Port5				Port9									
	2x2	Port1		Port3		Port5		Port7		Port9		Port11							
	1x2 + 2x1	Port1		Port3		Port4		Port5		Port7		Port8		Port9		Port11		Port12	
	4x1	Port1	Port2	Port3	Port4	Port5	Port6	Port7	Port8	Port9	Port10	Port11	Port12						
Y	1x4	Port1				Port5													
	2x2	Port1		Port3		Port5		Port7											
	1x2 + 2x1	Port1		Port3		Port4		Port5		Port7		Port8							
	4x1	Port1	Port2	Port3	Port4	Port5	Port6	Port7	Port8										
	1x2									Port9									
	2x1									Port9	Port10								

5
Main Func = PCH



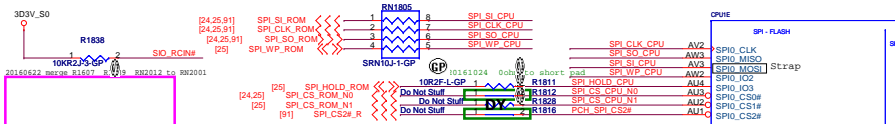
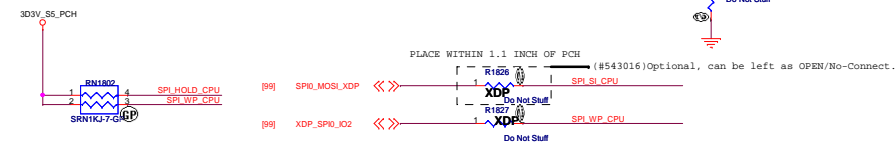
```
#543016 Rev0.7
1. VCCST_PWRGD is only 1.0 V tolerant.
2. VCCST_PWRGD must go low during Sx pwr states, regardless of the voltage level of VCCST
```

5
Main Func = PCH

PCH strap pin:

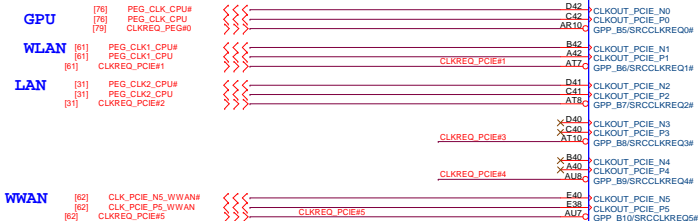
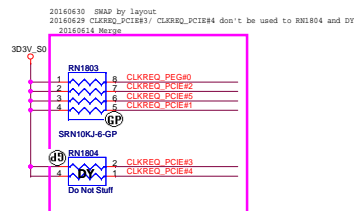
eSPI or LPC	Sampled at rising edge of RSMRST#
SML0ALERT# / GPP_C5	This signal has a weak internal pull-down. 0 = LPC is selected for EC. 1 = eSPI is selected for EC.

This signal has a weak internal pull-down.



```
0204 modfiv HDD PWR EN to T
```

RCIN#:
Frequency to Avoid: 33 MHz

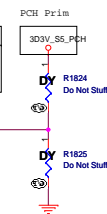


PCH strap pin:

BOOT HALT	
SPI0_MOSI	0 = ENABLED 1 = DISABLED WEAK INTERNAL PU

This signal has a weak internal pull-up.

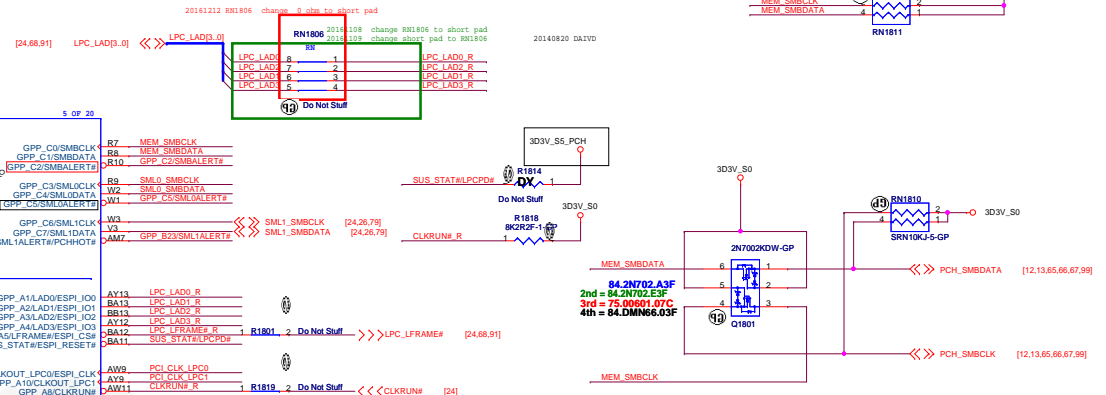
This signal has a weak internal pull-up



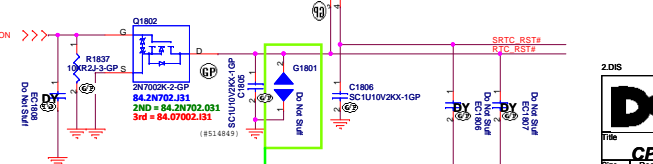
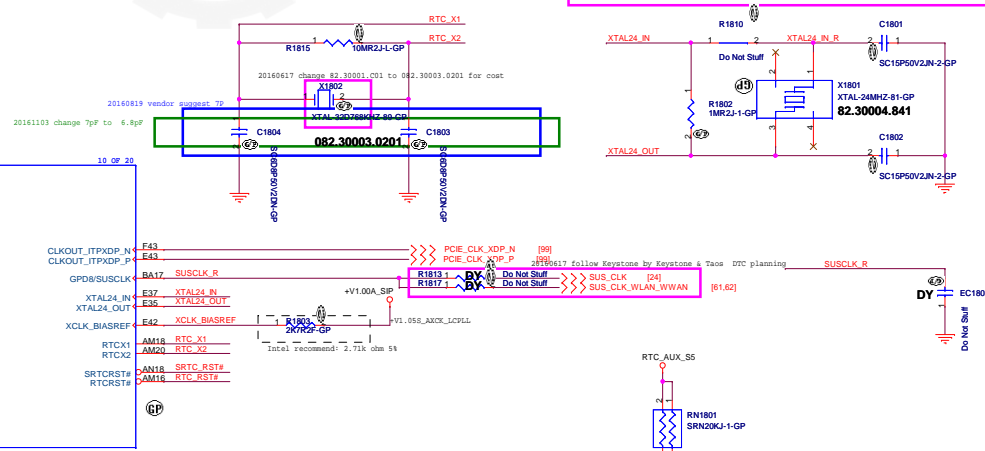
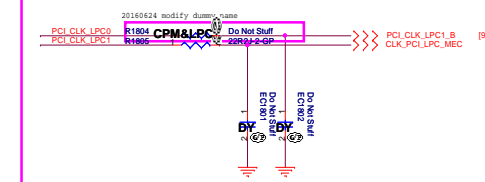
PCH strap pin:

No Reboot	Sampled at rising edge of PCH_PWROK
SMBALERT# / GPP_C2	<p>0 = Disable Intel ME Crypto Transport Layer Security (TLS) cipher suite (no confidentiality).</p> <p>1 = Enable Intel ME Crypto Transport Layer Security (TLS) cipher suite (with confidentiality). Must be pulled up to support Intel AMT with TLS and Intel SBA (Small Business Advantage) with TLS.</p>

The signal has a weak internal pull-down.



20160617 follow Vegas by Keystone & Taos DTC planning file



Layout: Place at the open door area

Main Func = PCH

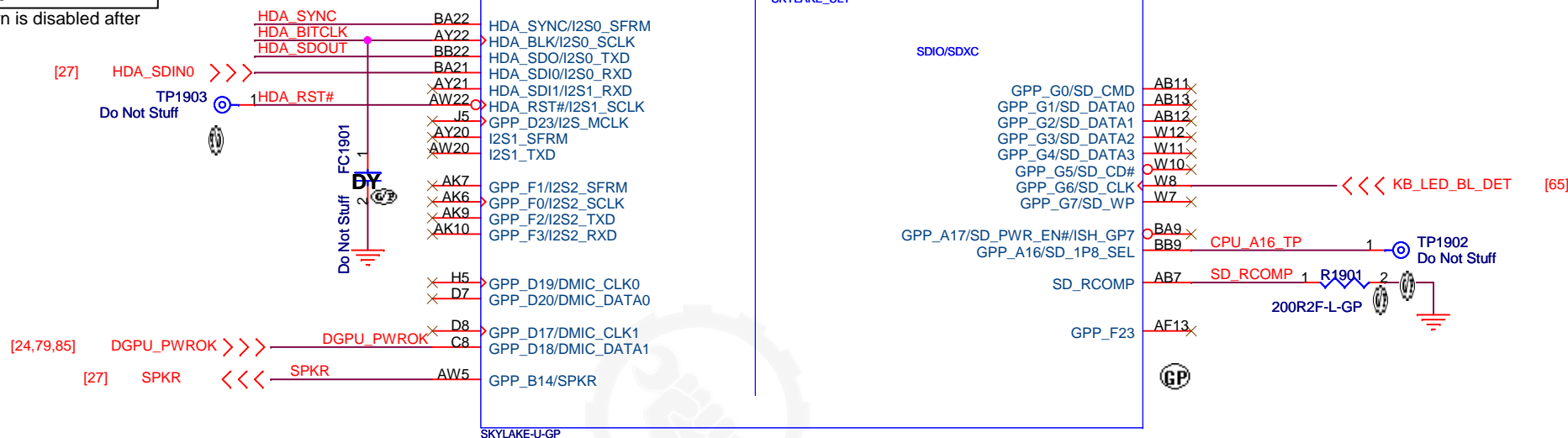
PCH strap pin:

Flash Descriptor Security Override/ Intel ME Debug Mode

HDA_SDOUT

Low = Default *
High = Enable

The internal pull-down is disabled after
PLTRST# deasserts



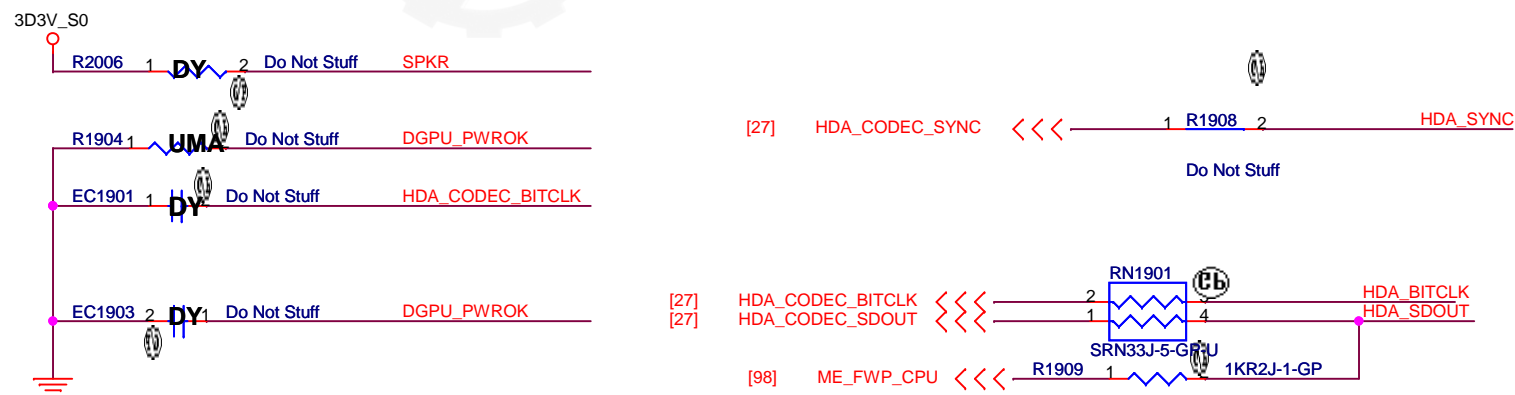
PCH strap pin:

NO REBOOT

HDA_SPKR

* Low = Enable (Default)
High = Disable

The internal pull-down is disabled after
PLTRST# deasserts



2.D/S



Wistron Corporation

21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title

CPU (AUDIO/SDIO/SDXC)

Size
A4

Document Number

Taos KBL-U

Rev
X00

Date: Monday, December 26, 2016

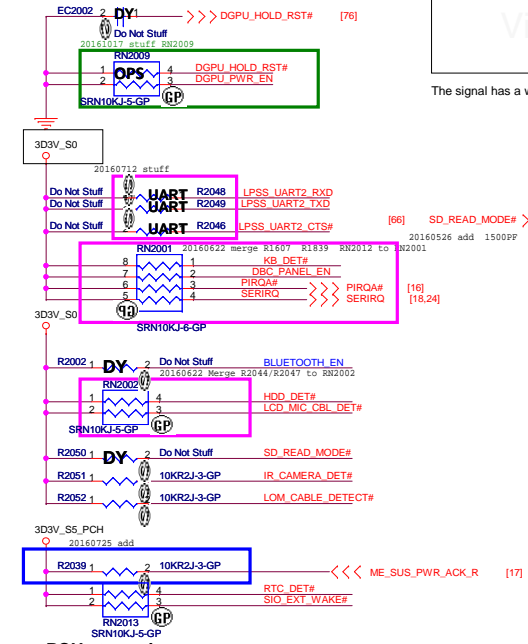
Sheet 19 of 105

Main Func = PCH

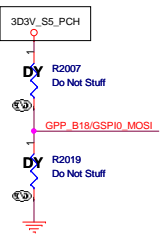
PCH strap pin:

No Reboot	Sampled at rising edge of PCH_PWROK
GSPH1_MOSI / GPP_B22	This field determines the destination of accesses to the BIOS memory range. Also controllable using Boot BIOS Destination bit (Chipset Configuration Registers: Offset 3410h:Bit 10). This strap is used in conjunction with Boot BIOS Destination Selection 0 strap. Bit 10 0 Boot BIOS Destination 1 SPI LPC

The signal has a weak internal pull-down.

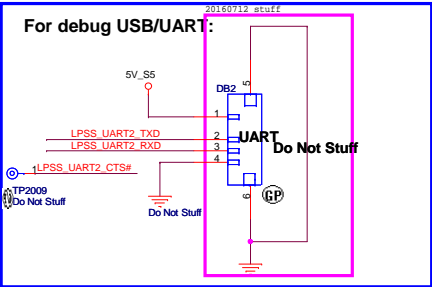


PCH Prim

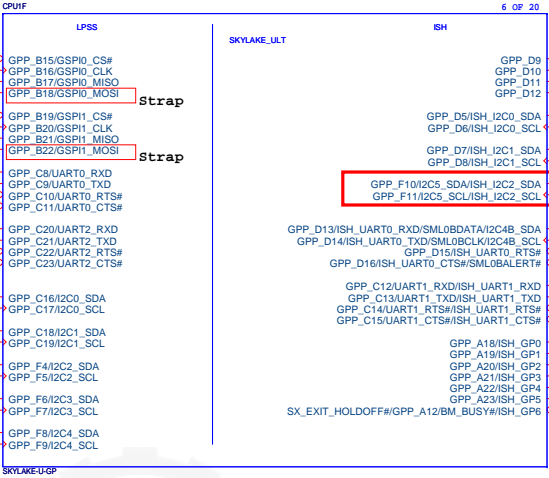


PCH strap pin:

No Reboot	Sampled at rising edge of PCH_PWROK
GSPH0_MOSI / GPP_B18	0 = Disable "No Reboot" mode. 1 = Enable "No Reboot" mode (PCH will disable the TCO Timer system reboot feature). This function is useful when running ITP/XDP. The signal has a weak internal pull-down.



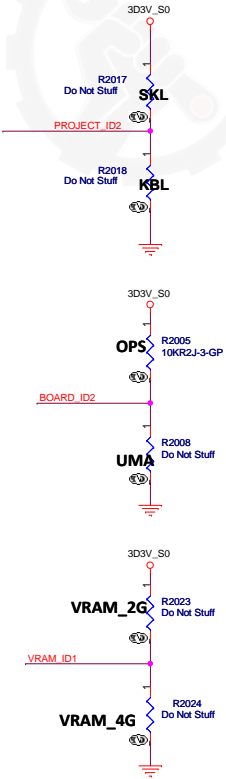
Intel has removed EHCI controller from BDW and proposed to use UART interface for Win7 debug.



(PDG#543016) Ensure that all I2C interface on-board terminations are pulled up to the same voltage rail as the device/end point.

BIOS strap pin:

BIOS VRAM Size Strap pin	PROJECT_ID2
KBL	0
SKL	1



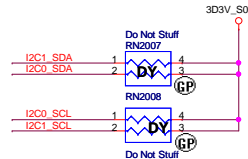
BIOS strap pin:

BIOS UMA/DIS Strap pin	BOARD_ID2
UMA	0
DIS	1

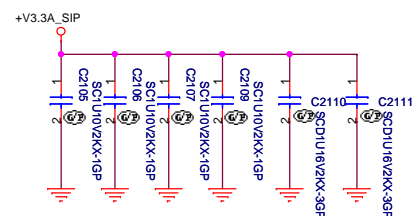
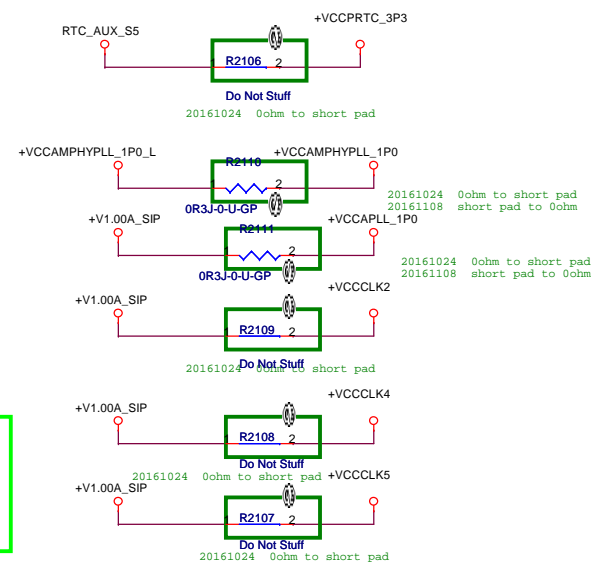
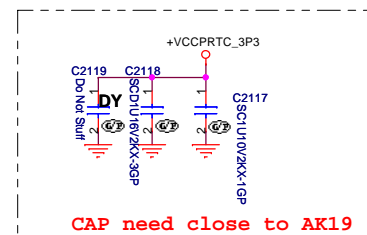
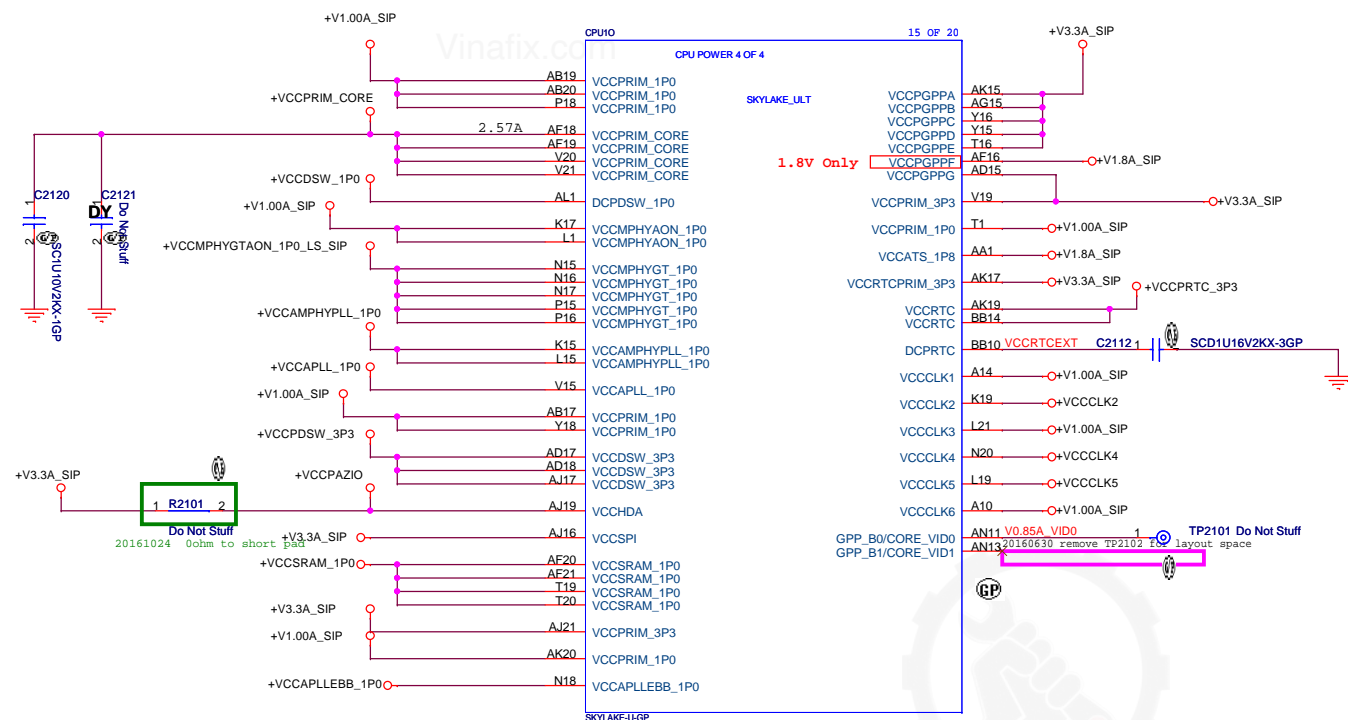
BIOS strap pin:

BIOS VRAM Size Strap pin	VRAM_ID1
4G	0
2G	1

(PDG#543016) If the UART/GPIO functionality is also not used, the signals can be left as no-connect.

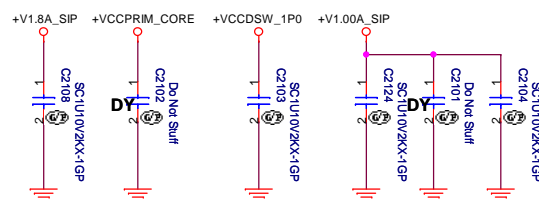


Main Func = PCH



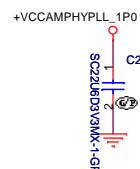
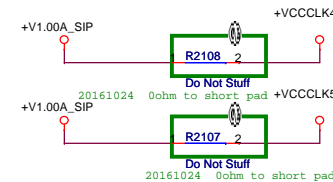
Layout Note:

1uF:
C2105 near V19
C2106 near AK17
C2107 near AG15
C2109 near Y16
C2110 near T16
C2111 near AJ19

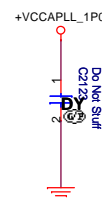


Layout Note:

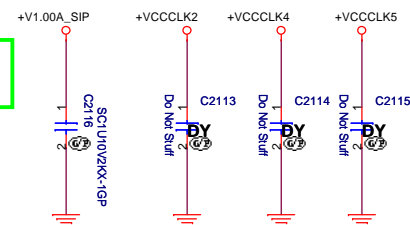
1uF:
C2101 near AB19
C2104 near K17
C2116 near A10
C2124 near AL1



Layout Note:
22uF:
C2122 near K15



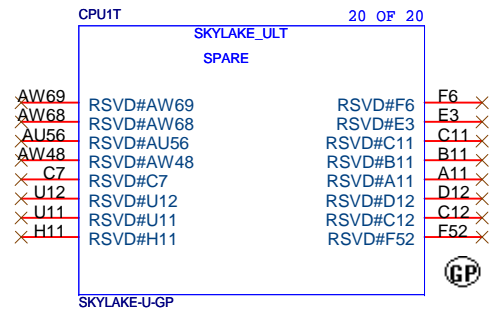
Layout Note:
22uF:
C2123 near K15




Layout Note:
1uF:
C2116 near A10
22uF:
C2115 near K19
C2114 near N20
C2113 near L19

Main Func = PCH

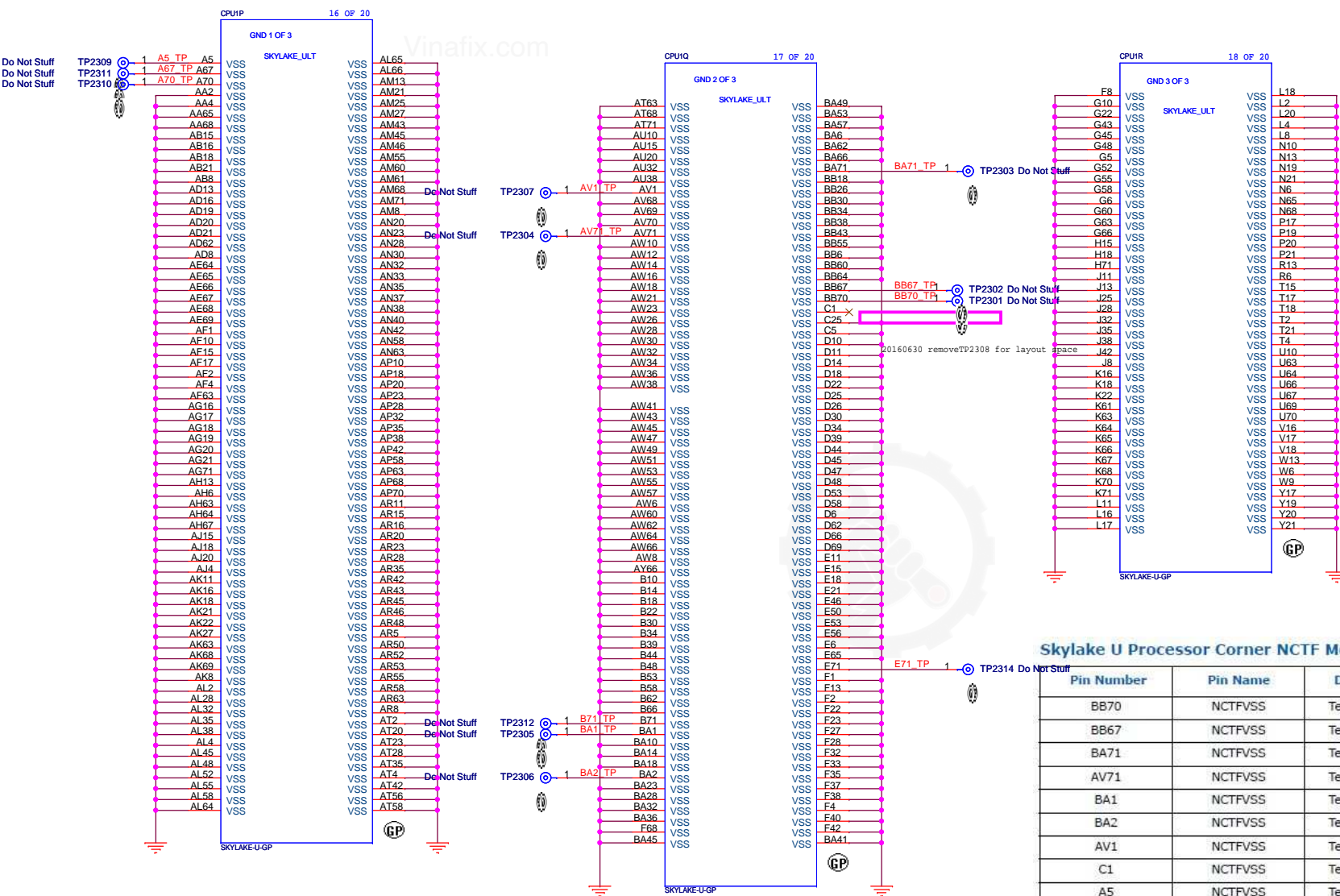
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2.DIS

		Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title CPU (RSVD)			
Size A4	Document Number Taos KBL-U		Rev X00
Date: Monday, December 26, 2016		Sheet 22 of	105


Main Func = PCH



Skylake U Processor Corner NCTF Motherboard Test Point Example

Pin Number	Pin Name	Description	Corner
BB70	NCTFVSS	Test Point (TP)	Corner BB71
BB67	NCTFVSS	Test Point (TP)	
BA71	NCTFVSS	Test Point (TP)	
AV71	NCTFVSS	Test Point (TP)	Corner BB1
BA1	NCTFVSS	Test Point (TP)	
BA2	NCTFVSS	Test Point (TP)	
AV1	NCTFVSS	Test Point (TP)	Corner A1
C1	NCTFVSS	Test Point (TP)	
A5	NCTFVSS	Test Point (TP)	
A70	NCTFVSS	Test Point (TP)	Corner A71
A67	NCTFVSS	Test Point (TP)	
B71	NCTFVSS	Test Point (TP)	
E71	NCTFVSS	Test Point (TP)	

2.DIS



Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title

CPU (VSS)

Size

A3

Document Number

Taos KBL-U

Rev

X00

Date:

Monday, December 26, 2016

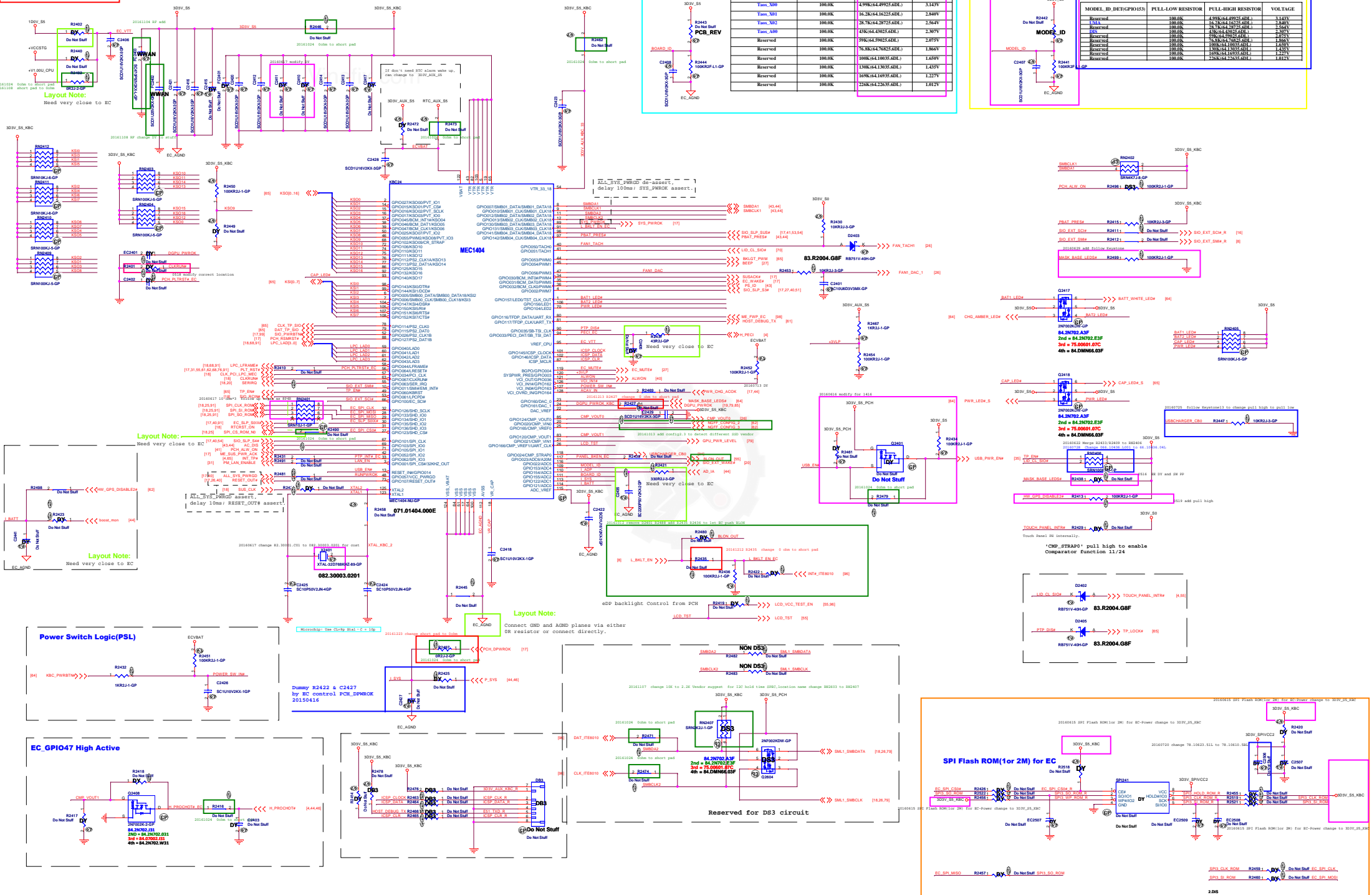
Sheet

23

of

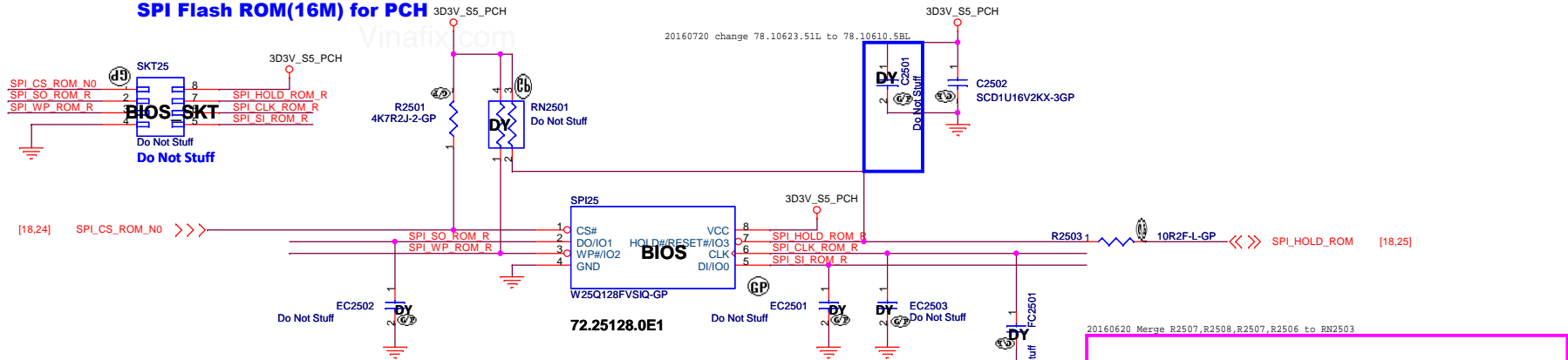
105

Main Func = KBC

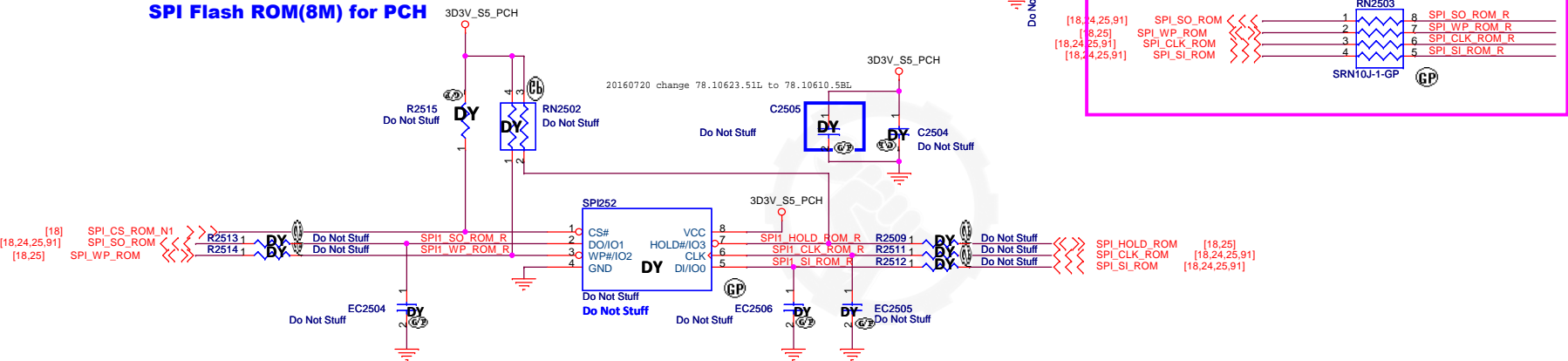


Main Func = SPI Flash

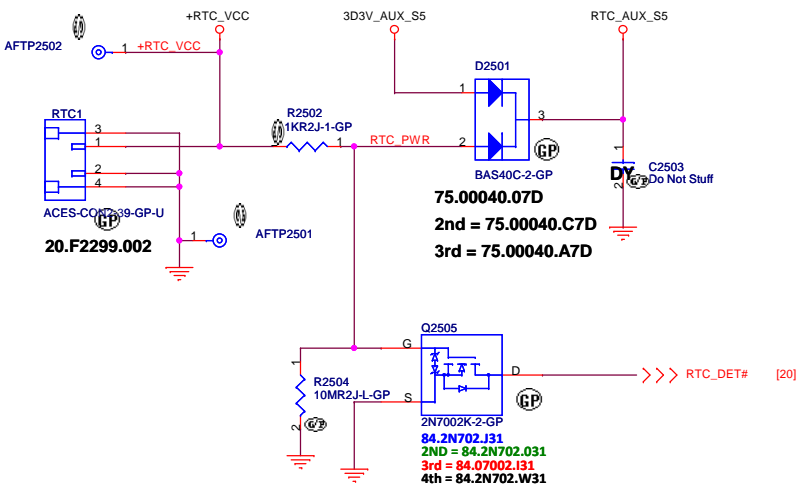
SPI Flash ROM(16M) for PCH



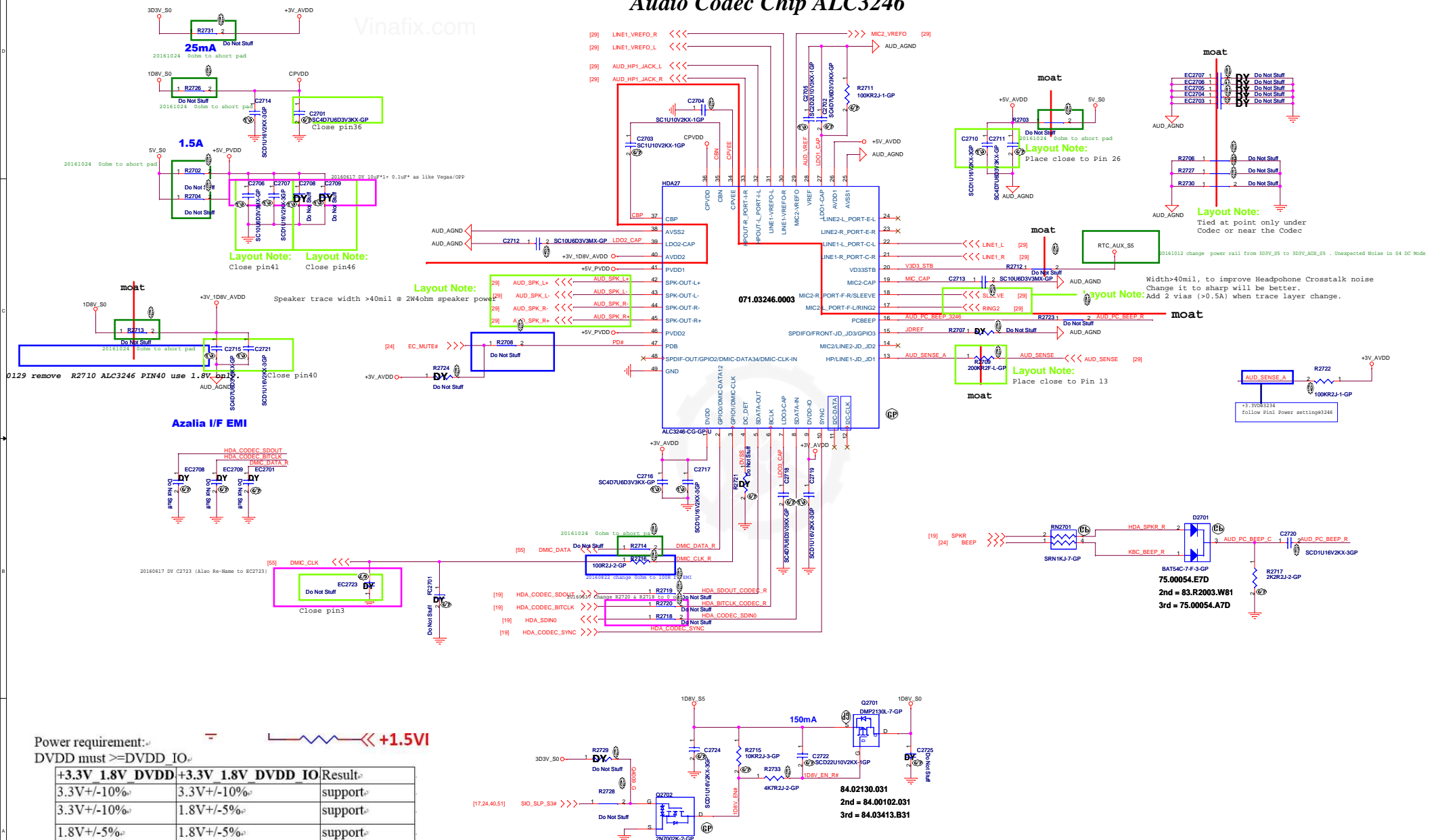
SPI Flash ROM(8M) for PCH



Main Func = RTC



Audio Codec Chip ALC3246



Power requirement:-


DVDD must \geq DVDD_IO.

+3.3V 1.8V DVDD	+3.3V 1.8V DVDD IO	Result
3.3V+/-10%	3.3V+/-10%	support
3.3V+/-10%	1.8V+/-5%	support
1.8V+/-5%	1.8V+/-5%	support
1.8V+/-5%	1.5V+/-5%	support
1.8V+/-5%	3.3V+/-10%	Not support

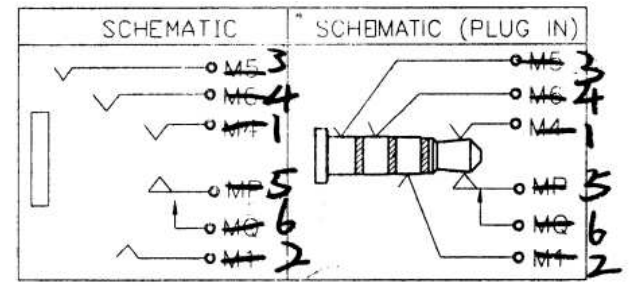
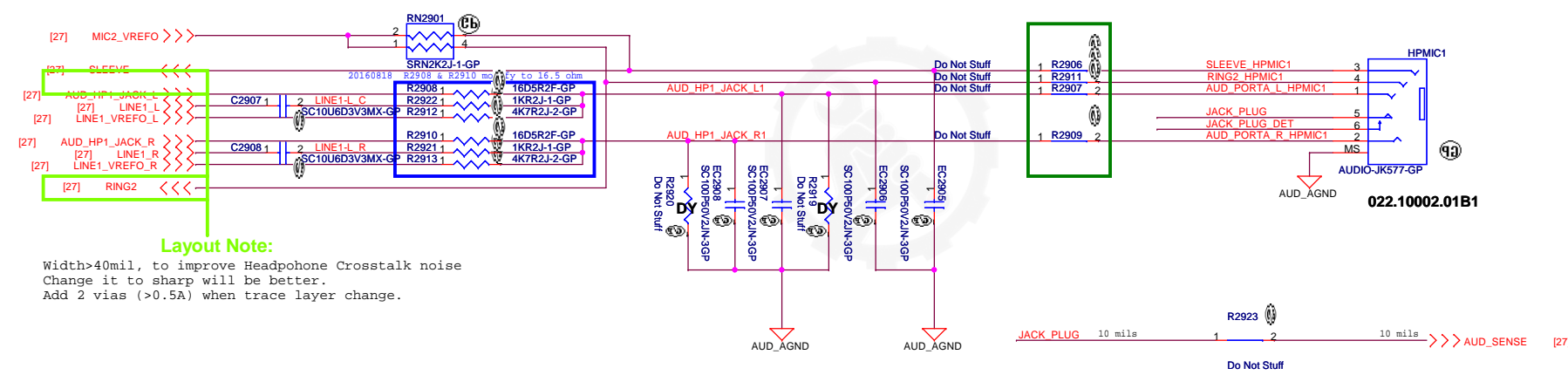
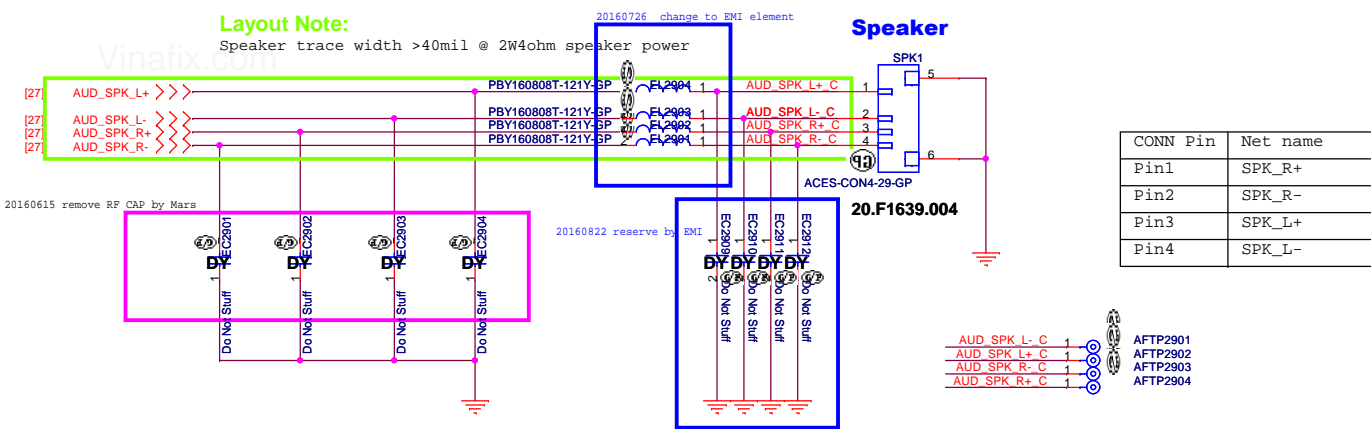
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Title (Reserved)			
Size A4	Document Number Taos KBL-U		Rev X00
Date: Monday, December 26, 2016		Sheet 28 of	105

Main Func = Audio




Main Func = Audio

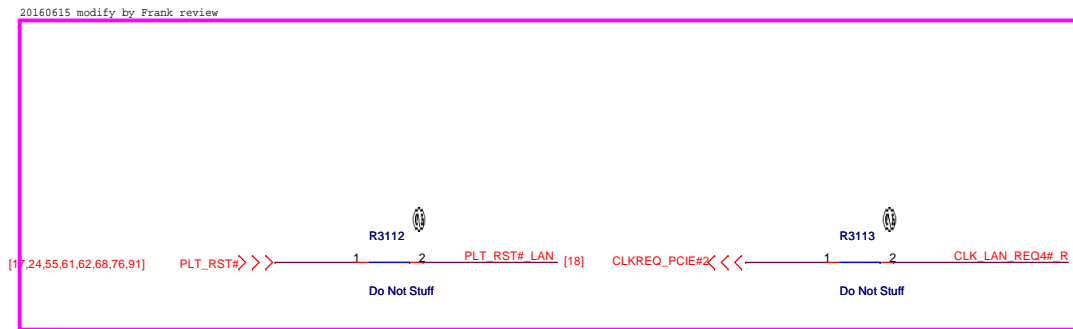
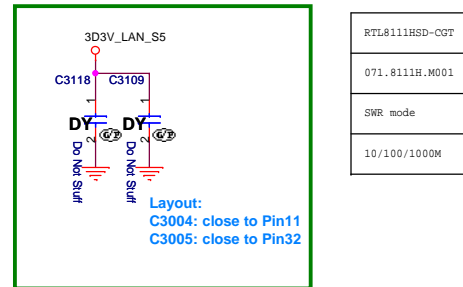
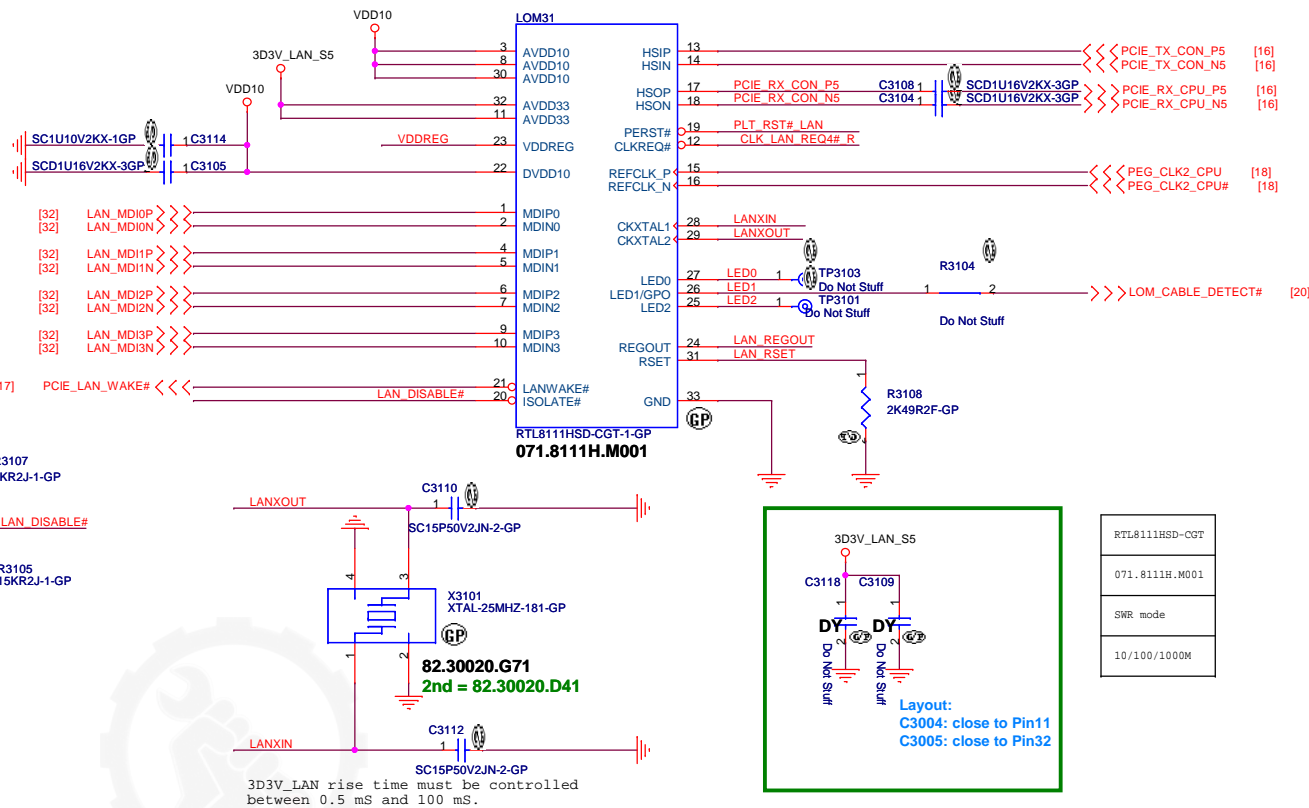
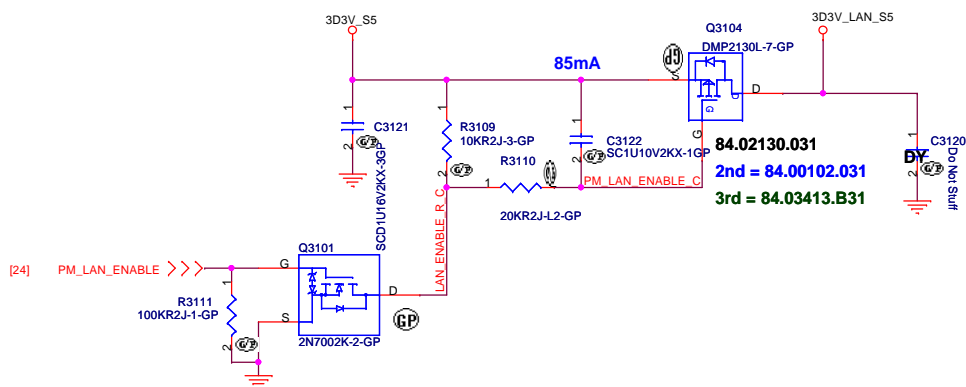
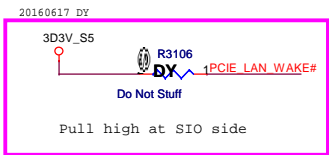
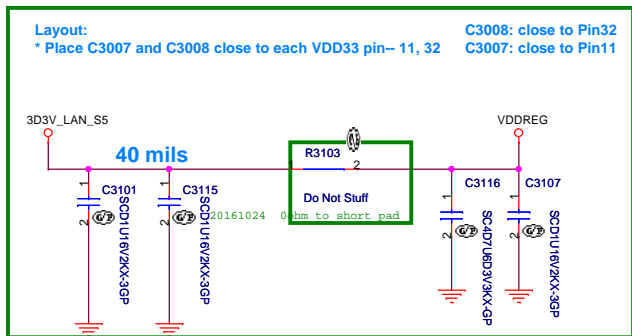
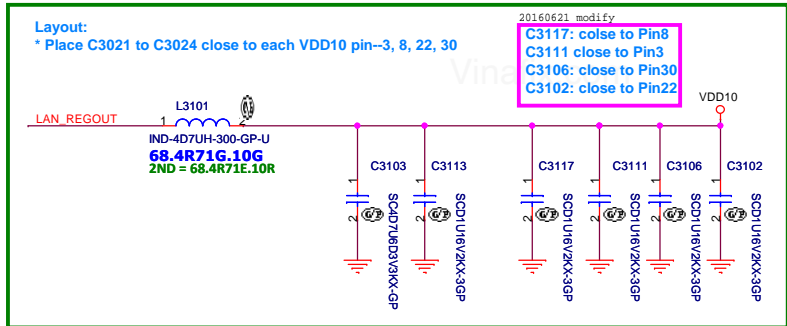
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(Blanking)

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Title (Reserved)			
Size A4	Document Number Taos KBL-U		Rev X00
Date: Monday, December 26, 2016		Sheet 30 of	105

Main Func = LAN

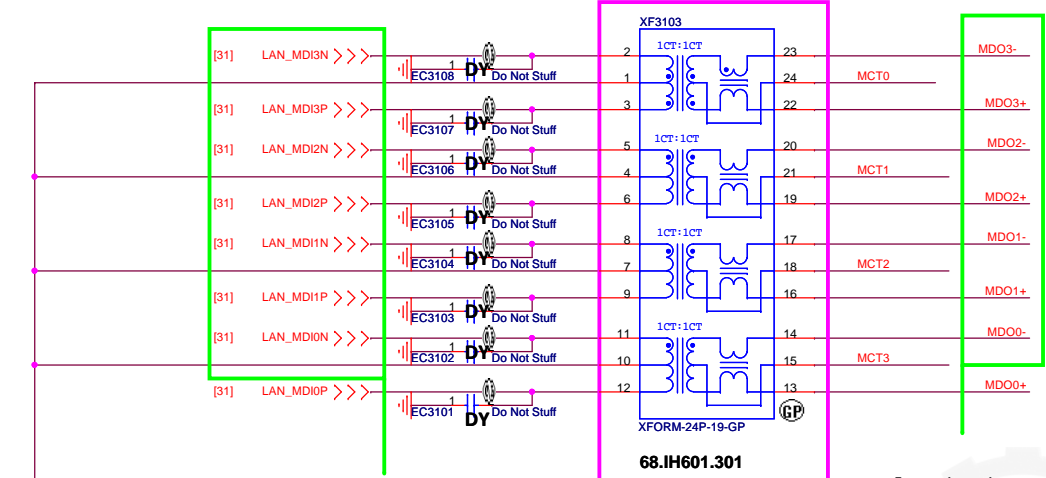


2.DIS

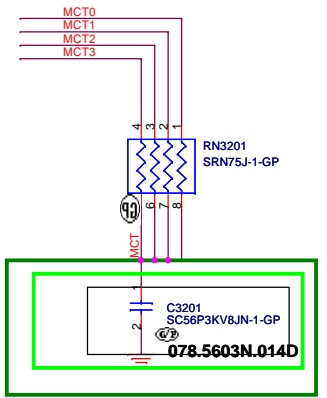
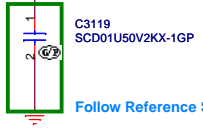
Main Func = LAN

LAN TransFormer (10/100/1000M)

20160706 change P/N 068.IH219.3001 to 68.IH601.301 because EMI fail

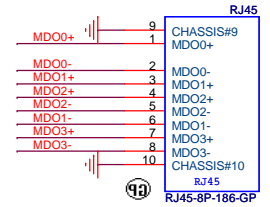
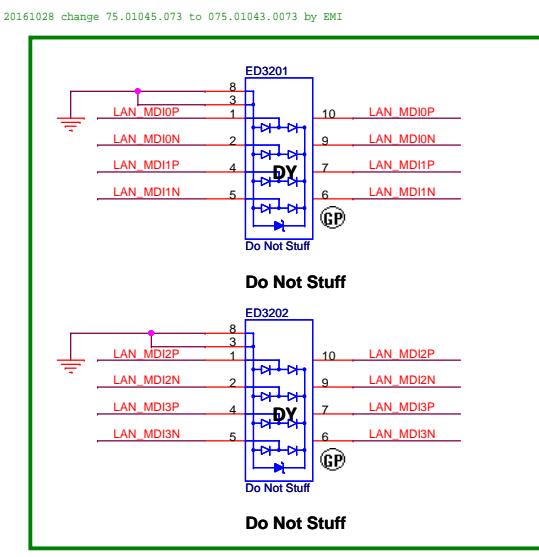


Layout note:
30 mil spacing between MDI differential pairs.



20161026 CAP change 078.5603N.0141 to 078.5603N.014D

Layout note:
30 mil spacing between MDI differential pairs.



022.10001.0D41

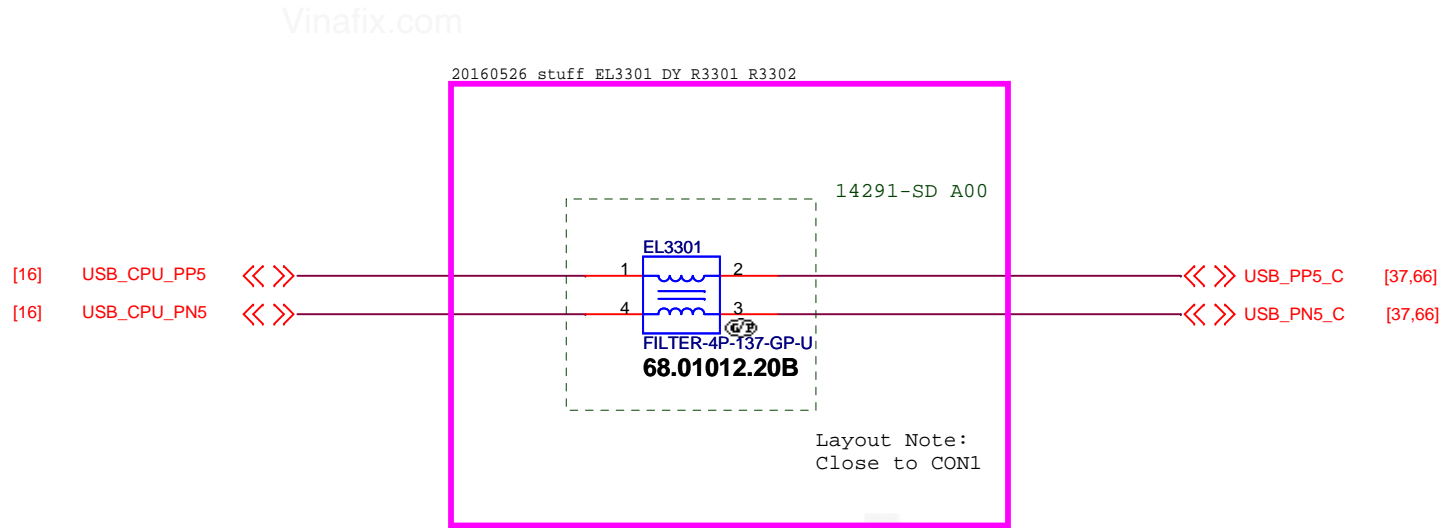
RJ45

Main : 022.10001.0D41


2nd : 022.10001.0C41

2.DIS

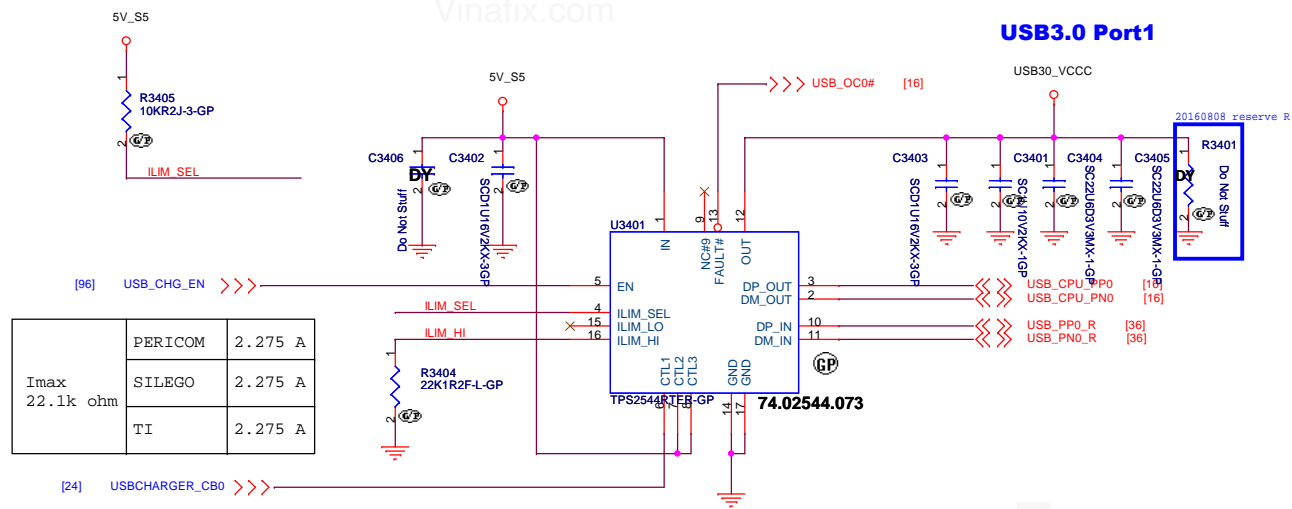
Main Func = Card Reader



2.DIS

		Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title Card Reader-RTS5170			
Size A4	Document Number Taos KBL-U		Rev X00
Date: Monday, December 26, 2016		Sheet 33 of	105

Main Func = USB2.0 Port3



PI5USB2544 Device Control Pins Truth Table

CTL1	CTL2	CTL3	ILIM_SEL	MODE	Current Limit Setting	Comment
0	0	0	0	Discharge	NA	OUT held low
0	0	0	1	Discharge	NA	
0	x	1	x	DCP_Auto	ILIM_HI	Data lines disconnected
0	1	0	0	SDP1	ILIM_LO	Data lines connected
0	1	0	1	SDP1	ILIM_HI	
0	1	1	0	DCP_Auto	ILIM_HI	Data lines disconnected
0	1	1	1	DCP_Auto	ILIM_HI	Data lines disconnected
1	0	0	0	DCP_Shorted	ILIM_LO	Device forced to stay in DCP BC1.2 charging mode
1	0	0	1	DCP_Shorted	ILIM_HI	
1	0	1	0	Divider-1A	ILIM_LO	Device forced to stay in Divider-1A charging mode
1	0	1	1	Divider-1A	ILIM_HI	
1	1	0	0	SDP1	ILIM_LO	
1	1	0	1	SDP1	ILIM_HI	Data lines connected
1	1	1	0	SDP2 ⁽¹⁾	ILIM_LO	
1	1	1	1	CDP ⁽¹⁾	ILIM_HI	Data lines connected

Note:
(1) No OUT discharge when changing between 1111 and 1110.

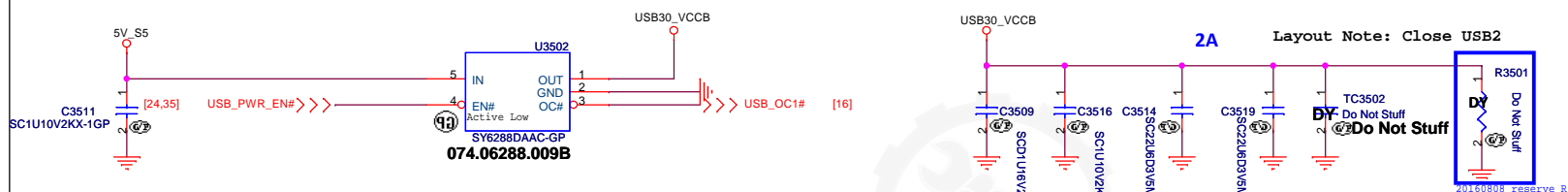
Main Func = USB3.0 Port1

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USB3.0 Port1

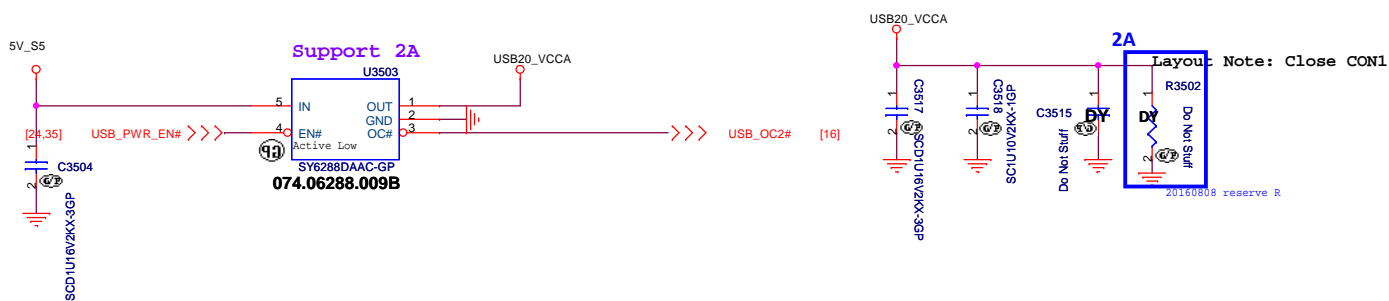
Main Func = USB3.0 Port2

USB3.0 Port2



Main Func = USB2.0 Port3

USB2.0 Port3 (IO Board)

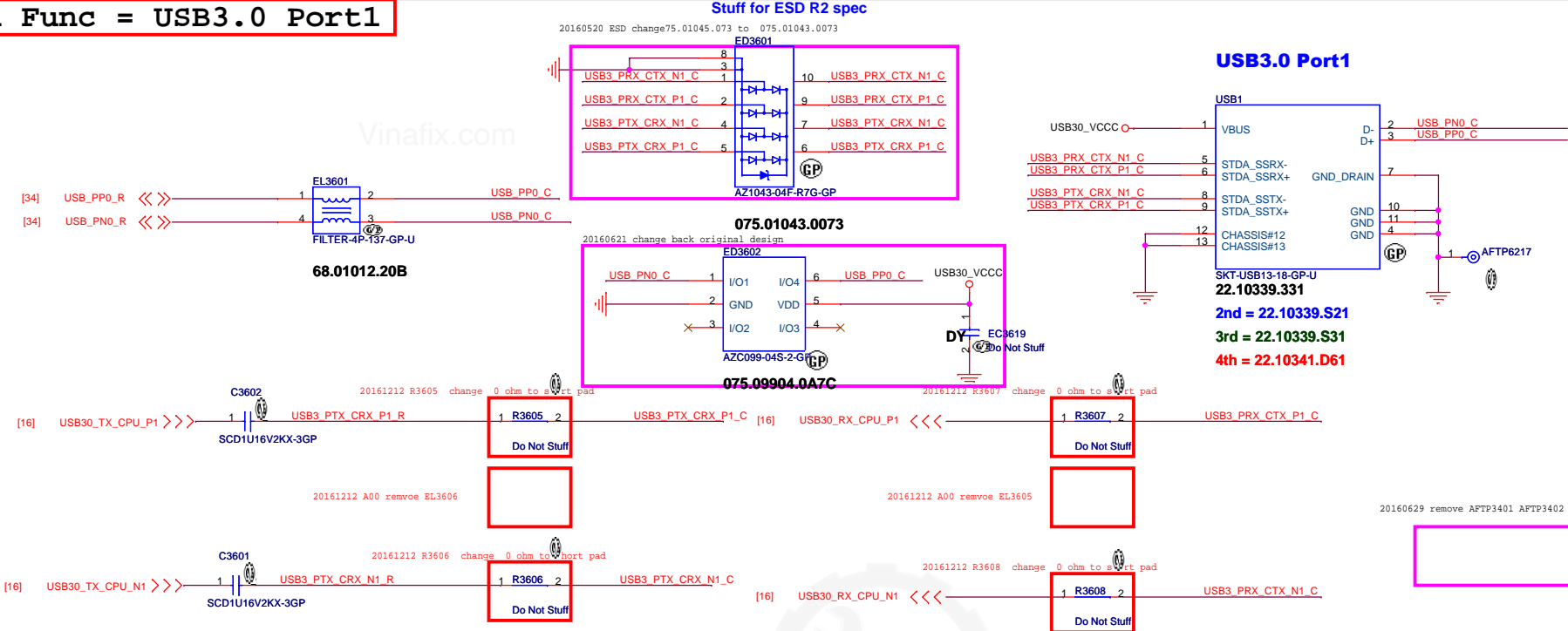


2.DIS

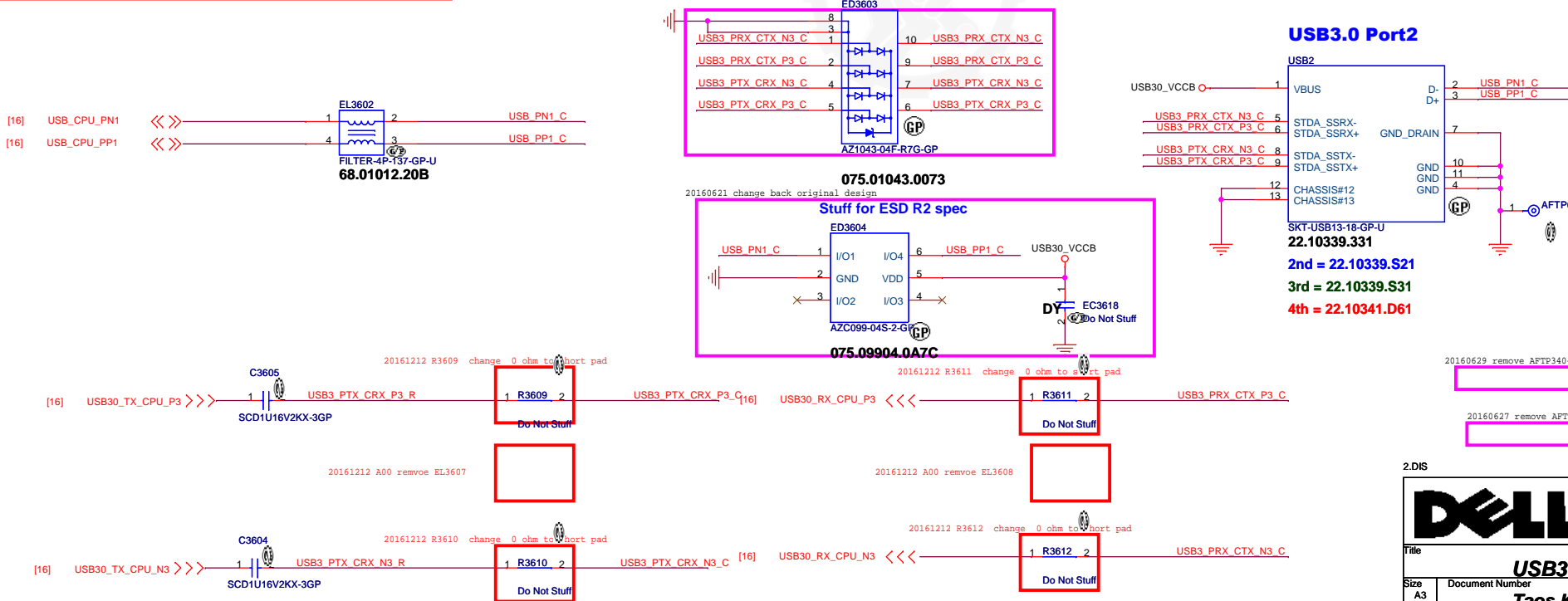
DELL Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **USB switch**
Size: Document Number: **Taos KBL-U** Rev: **X00**
Date: Monday, December 26, 2016 Sheet: 35 of 105

Main Func = USB3.0 Port1



Main Func = USB3.0 Port2



DELL Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

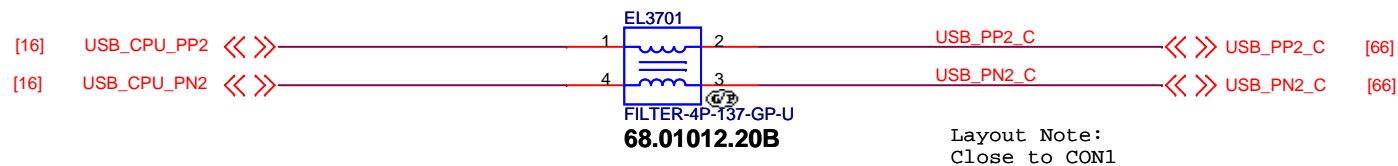
Title **USB30**

Size A3 Document Number **Taos KBL-U** Rev **X00**

Date: Monday, December 26, 2016 Sheet 36 of 105

Vinafix.com

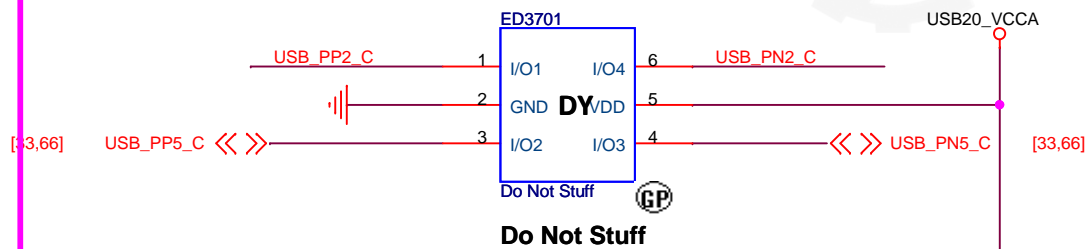
USB3 (USB2.0) CMC



20160615 DY ED3701 by EMI

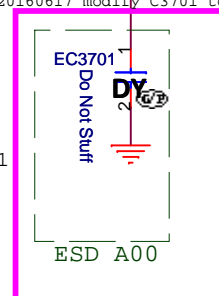
USB ESD Diode

Stuff for ESD R2 spec



20160617 modify C3701 to EC3701 and DY

Layout Note:
Close to CON1



2.DIS

DELL		Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title USB20			
Size A4	Document Number Taos KBL-U		Rev X00
Date: Monday, December 26, 2016		Sheet 37 of 105	


Main Func = USB3.0 Port1

Vinafix.com

(Blanking)



2.DIS

		Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title (Reserved)			
Size A4	Document Number Taos KBL-U		Rev X00
Date: Monday, December 26, 2016		Sheet 38 of	105


Main Func = USB3.0 Port1

Vinafix.com

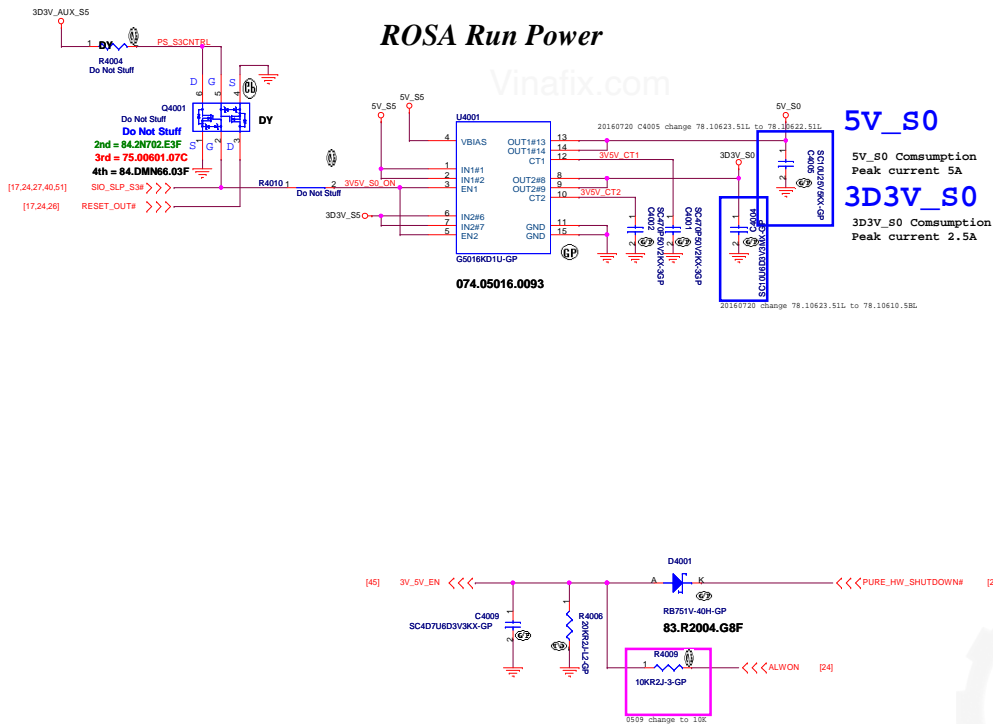
(Blanking)



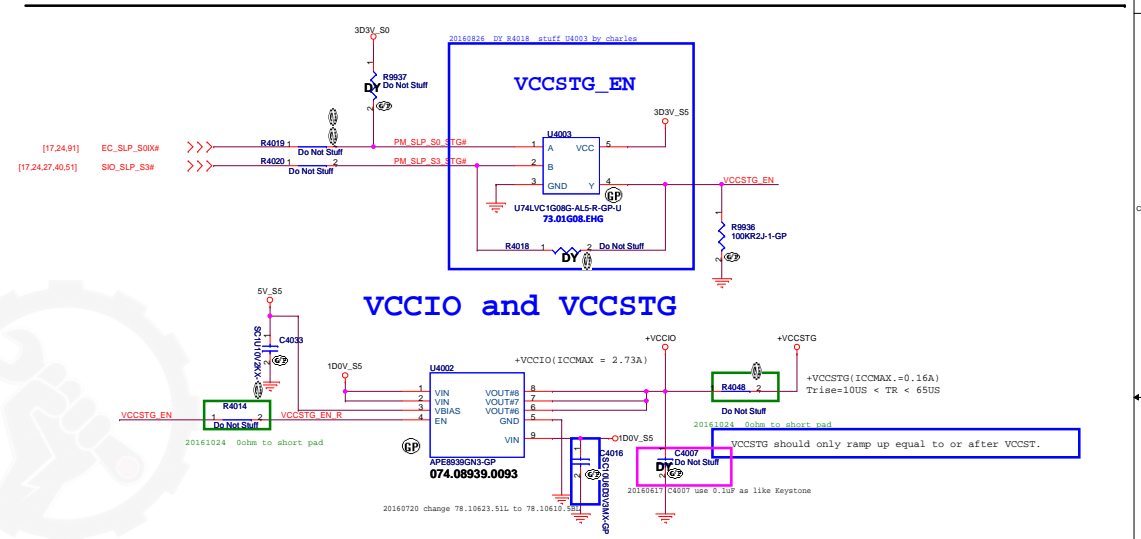
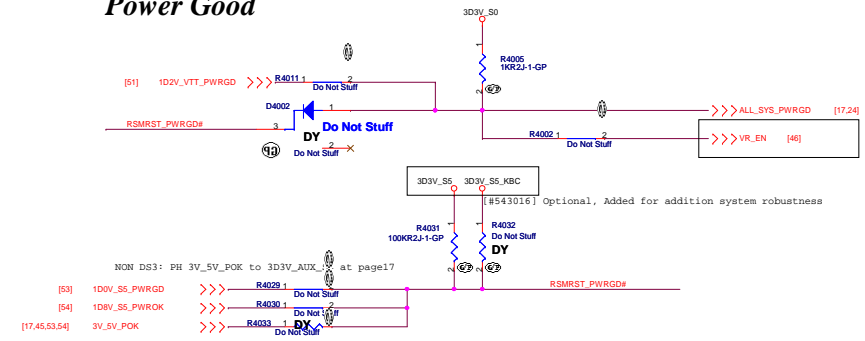
2.DIS

		Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title (Reserved)			
Size A4	Document Number Taos KBL-U		Rev X00
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ROSA Run Power



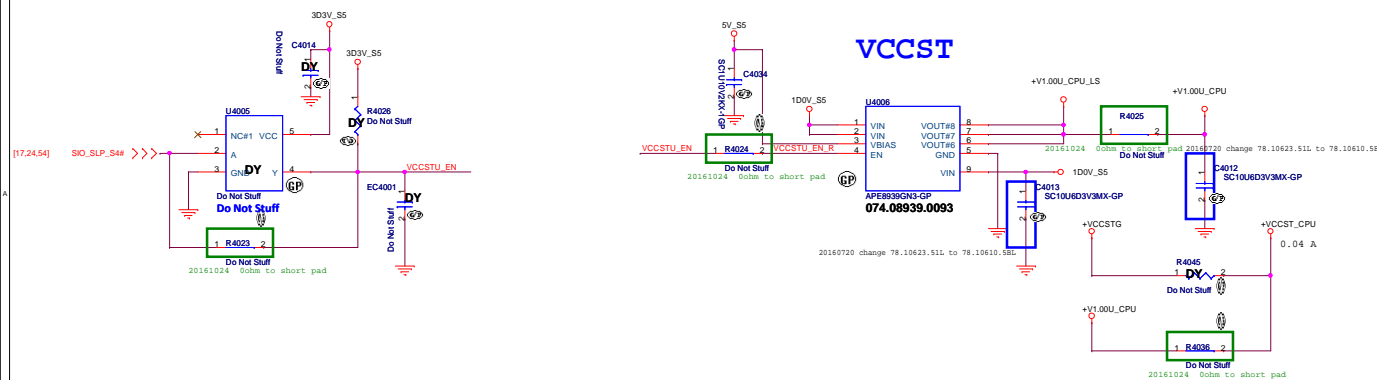
Power Good



EOPIO and EDRAM

MANAGEMENT RAIL POWER GENERATION

VCCST, VCCSTG, and VCCPLL can remain powered during S4 and S5 power states for board VR optimization.




20160630 remove , ALL 1D8V_S5 to +V1.8A

V1.8S

Main Func = Power Plane & Sequence



 <div style="display: inline-block; vertical-align: middle; margin-left: 10px;"> Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C. </div>		
Title <div style="text-align: center; font-size: 1.2em; font-weight: bold;"> <i>Connected_Standby(1/2)+DS3</i> </div>		
Size A4	Document Number <div style="text-align: center; font-size: 1.2em; font-weight: bold;"> <i>Taos KBL-U</i> </div>	Rev <div style="text-align: center; font-size: 1.2em; font-weight: bold;"> <i>X00</i> </div>
Date: Monday, December 26, 2016		Sheet 41 of 105


Main Func = DIMM1
Main Func = DIMM2

Vinafix.com

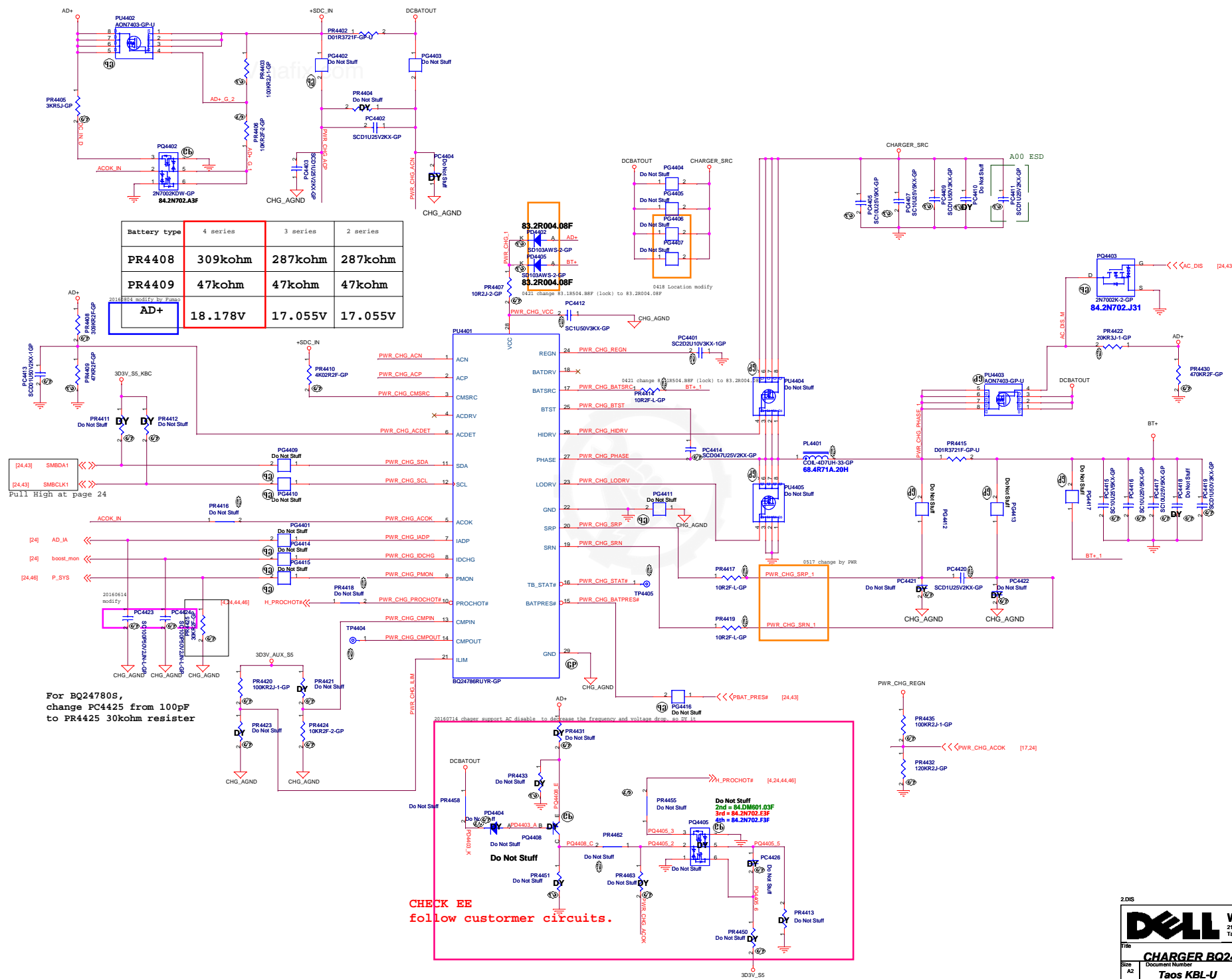
VREF CIRCUITRY

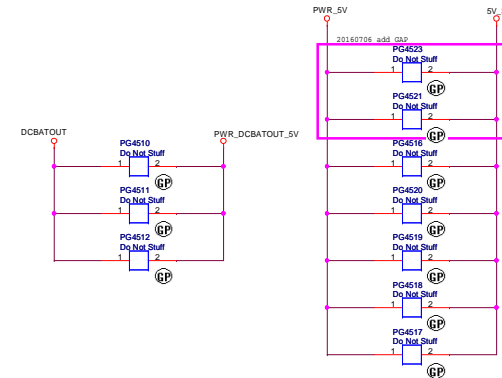
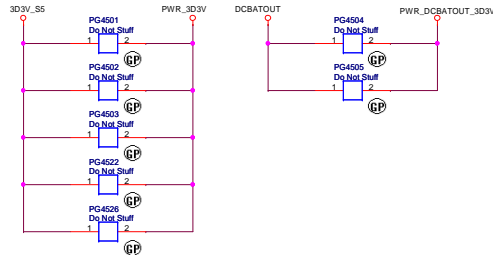
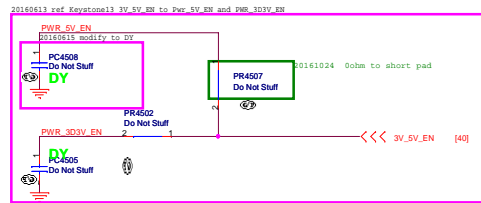


2.DIS

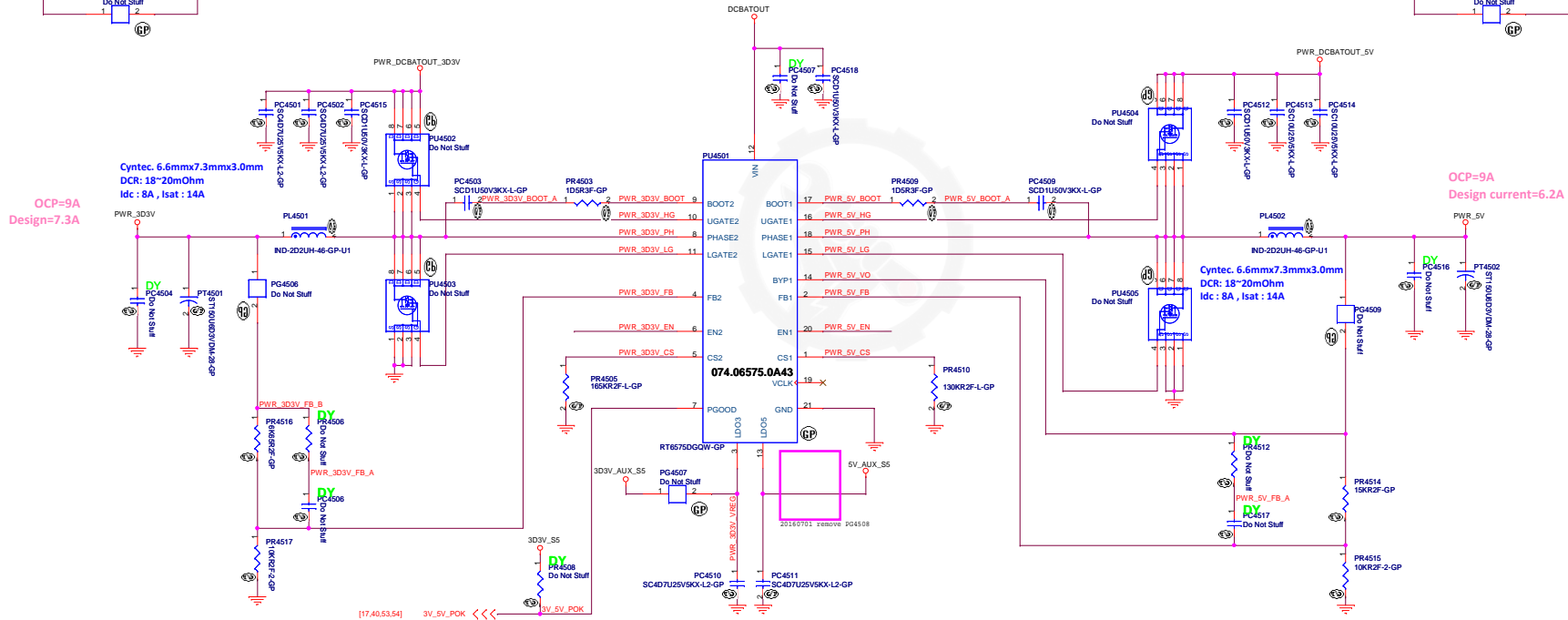
		Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title Connected_Standby(2/2)		
Size A4	Document Number Taos KBL-U	Rev X00
Date: Monday, December 26, 2016		Sheet 42 of 105

Main Func = Charger



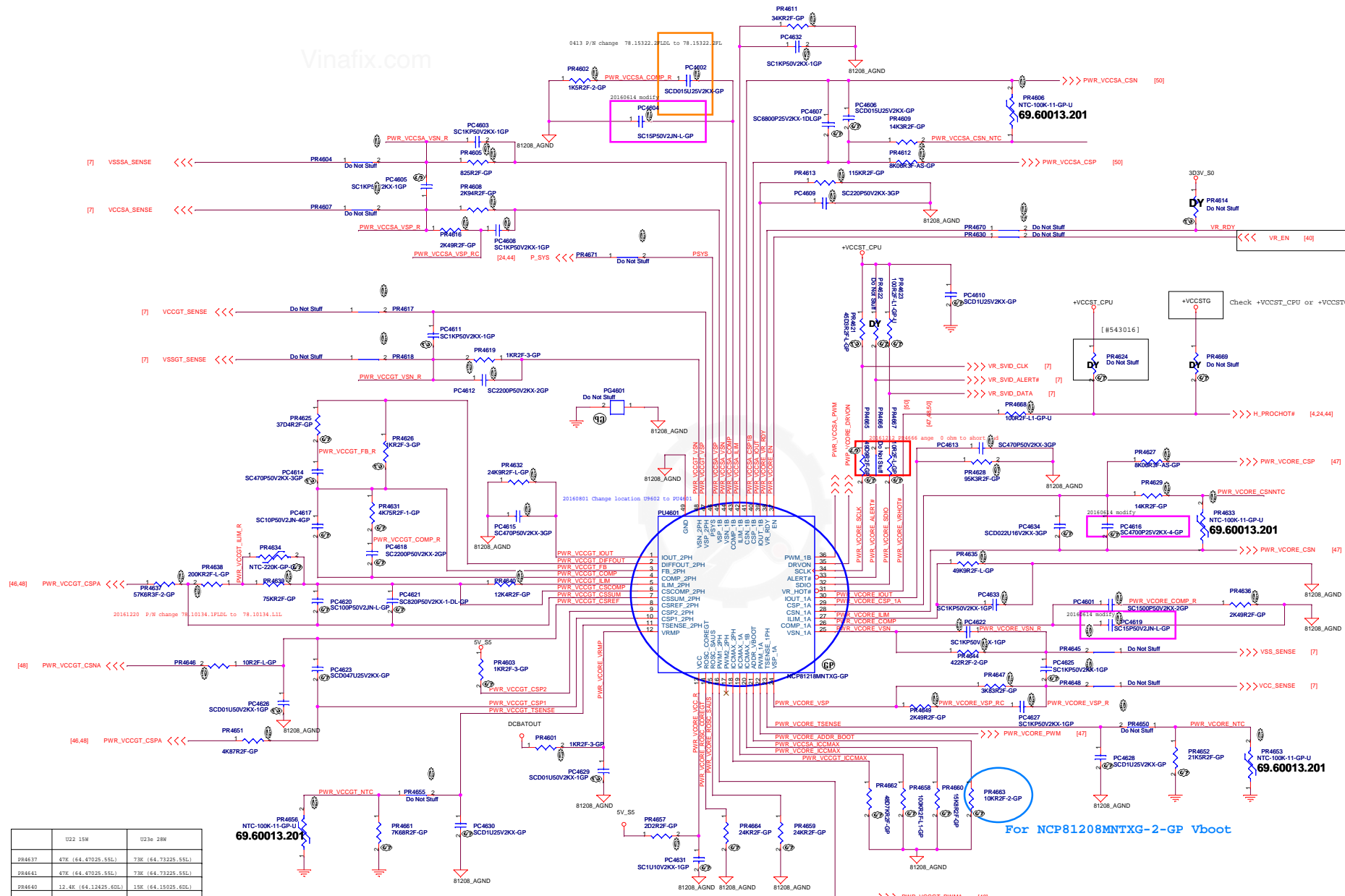


Pin to Pin TPS51275B
074.51275.0C73




2.0S

Vinafix.com

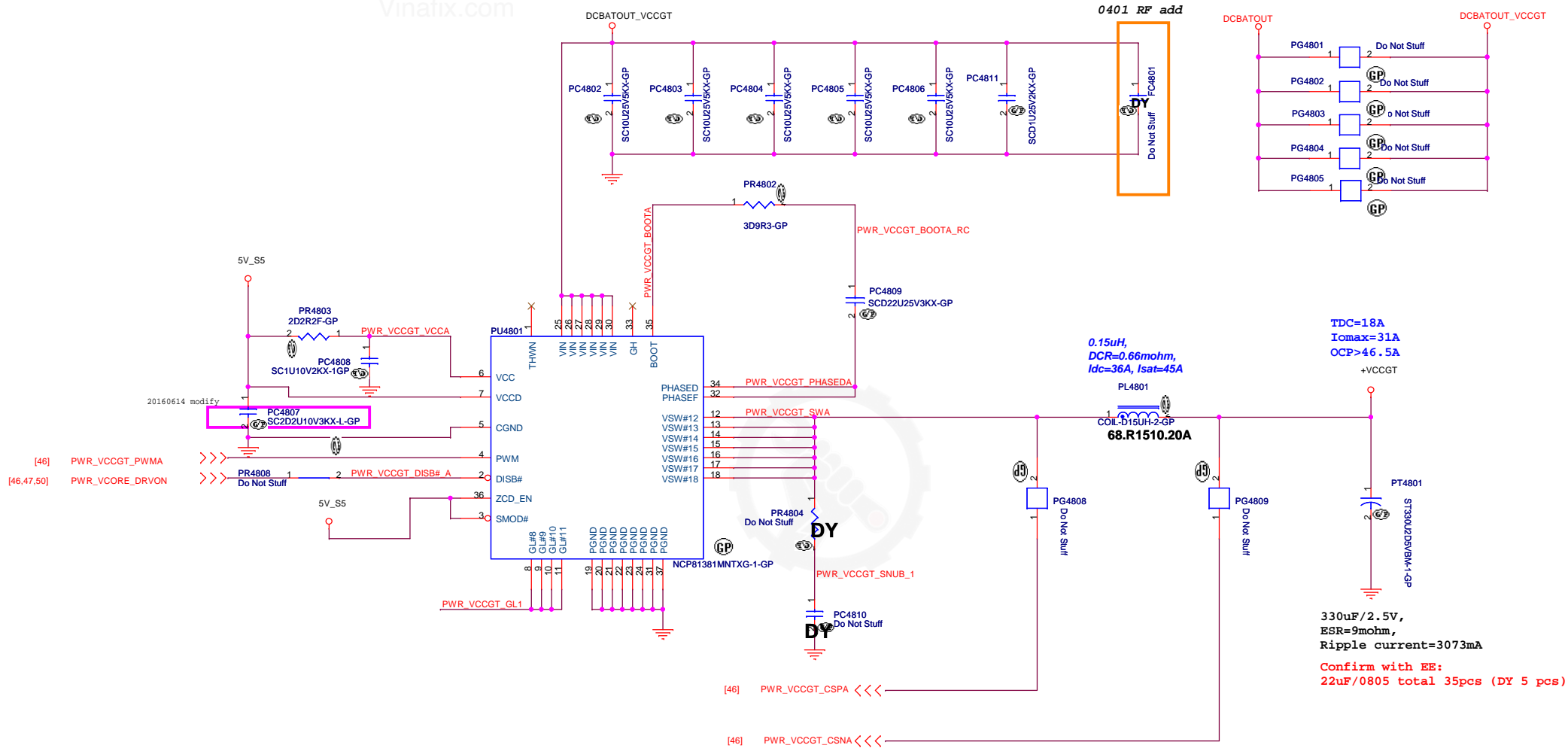


	U22 15W	U23a 28W
PR4637	47K (64.47025, 55L)	73K (64.73225, 55L)
PR4641	47K (64.47025, 55L)	73K (64.73225, 55L)
PR4640	12.4K (64.12425, 60L)	15K (64.15025, 60L)
PR4652	69.9K (64.69925, 60L)	88.7K (64.88725, 60L)
PR4658	88.7K (64.88725, 60L)	90.9K (64.90925, 60L)
PR4647	2.37K (64.23715, 60L)	2.15K (64.21515, 60L)
PR4635	18.3K (64.38325, 60L)	37.4K (64.37425, 60L)
PR4628	73.2K (64.73225, 60L)	69.8K (64.69825, 60L)

For NCP81208MNTXG-2-GP Vboot

		Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title <i>NCP81382MN_CPU_VCORE(2/3)</i>			
Size A3	Document Number <i>Taos KBL-U</i>	Rev <i>X00</i>	
Date: <i>Monday, December 26, 2016</i>	Sheet <i>47</i>	of <i>105</i>	

```
Main Func = CPU_CORE
```



2.DIS




Main Func = CPU_CORE

Vinafix.com

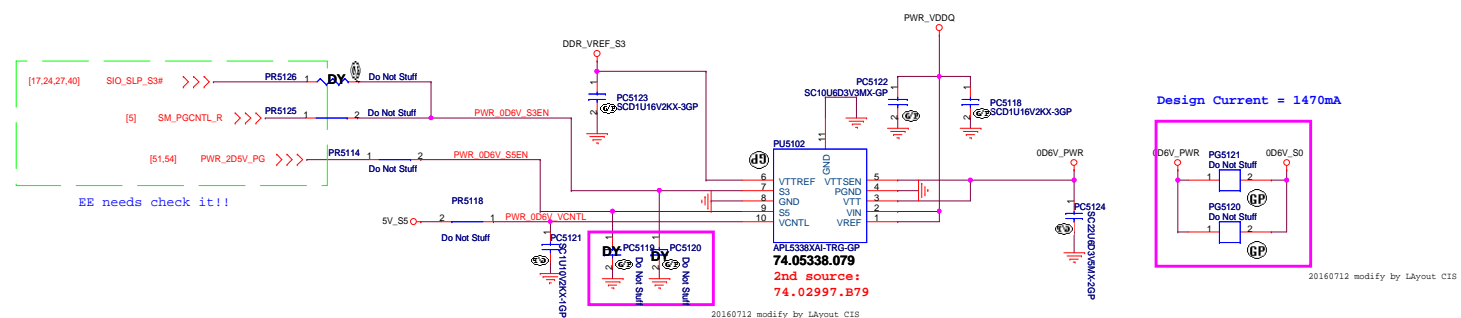
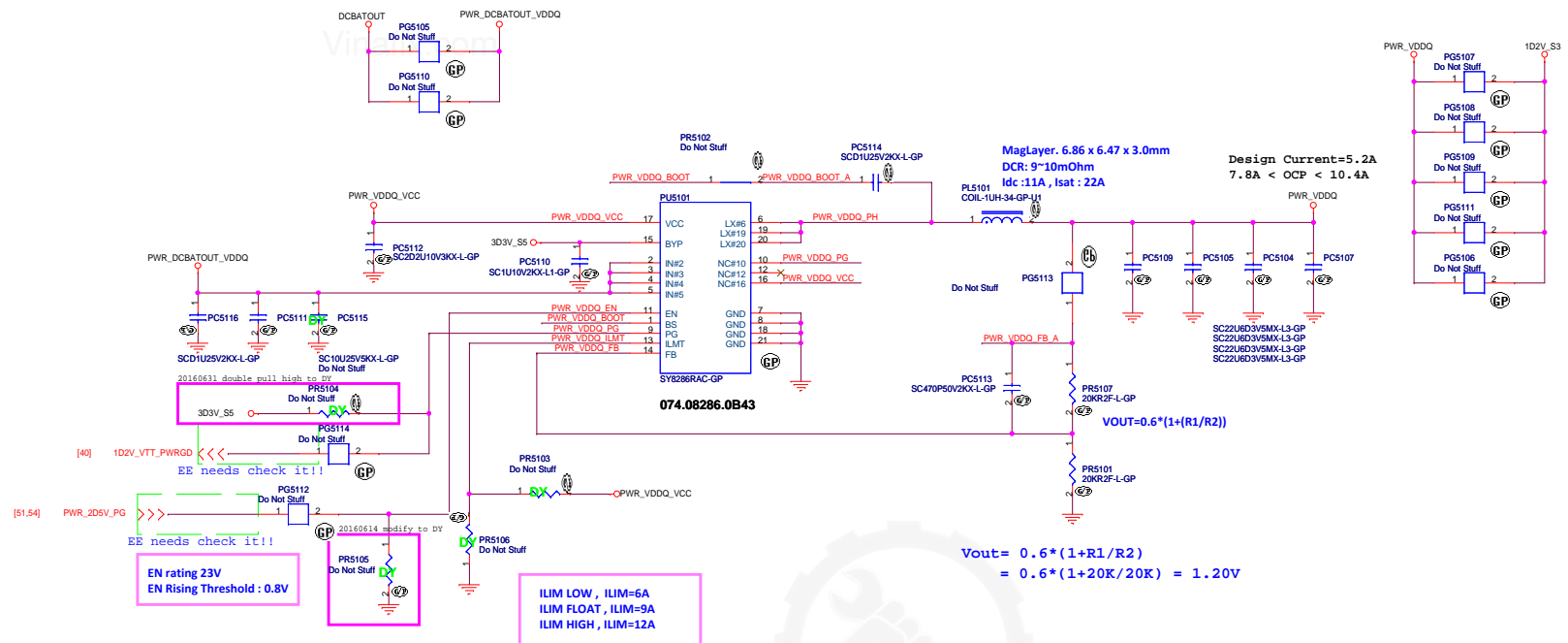
(Blanking)



2.DIS

		Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title NCP81210MN_CPU_VCCGTUS			
Size A4	Document Number Taos KBL-U		Rev X00
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Main Func = VDDQ



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2.DIS



Wistron Corporation
21F, 6th, Sec. 1, Hsin Tsa Yiu Rd., Hsichia,
Taipei Hsien 221, Taiwan, R.O.C.

Title

DCDC-0D975V_VCCIO

Size

A2

Document Number

Taos KBL-U

Rev

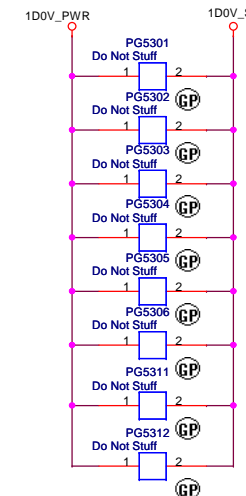
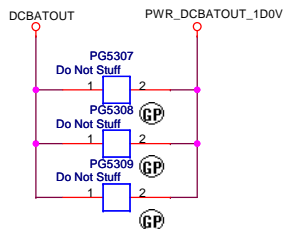
X00

Date: Monday, December 26, 2016

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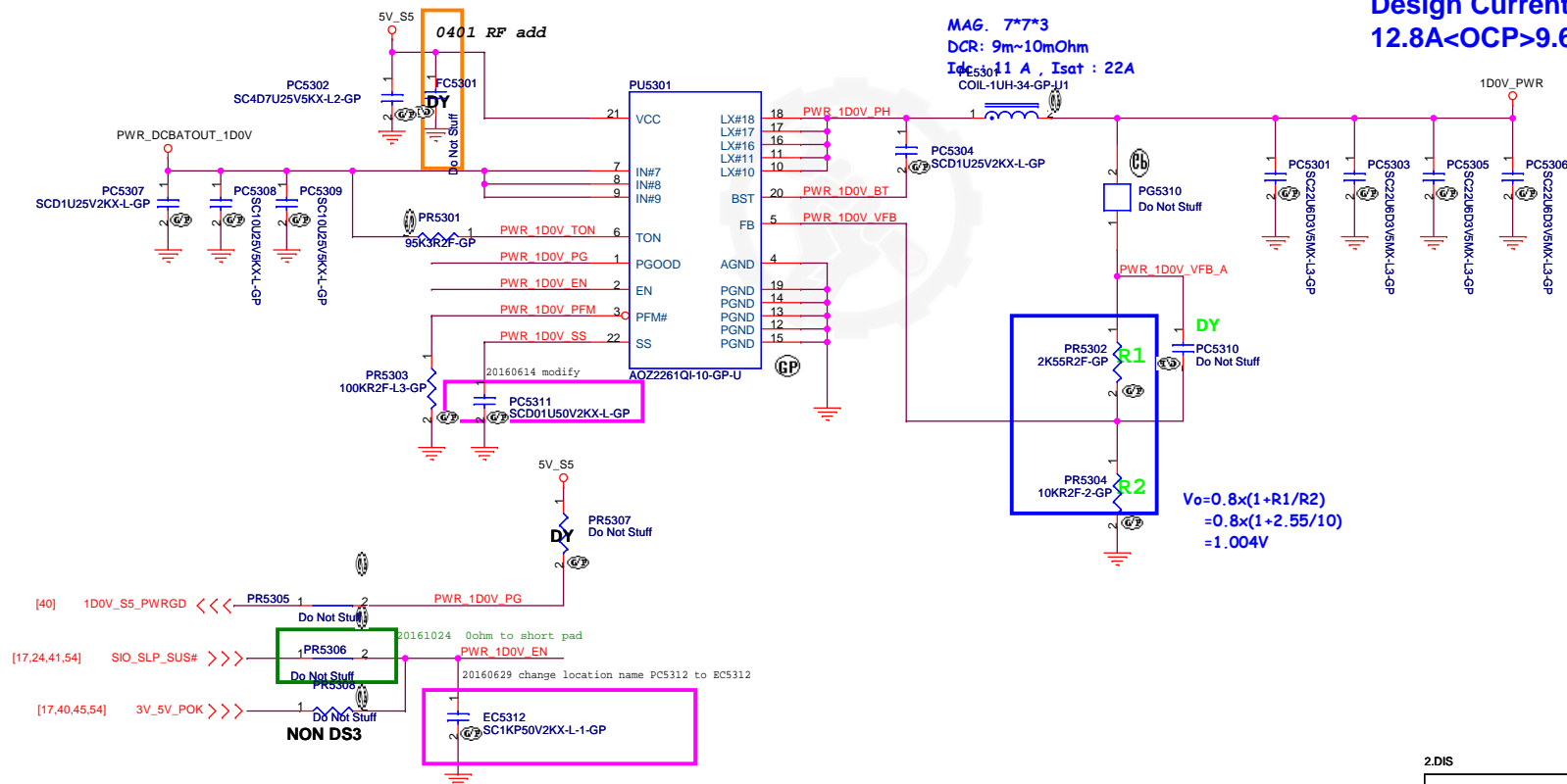
Main Func = 1D0V

Vinafix.com



AOZ2261 for 1D0V

Design Current : 6.4A
12.8A < OCP > 9.6A



2.DIS

APL5930 for DDR4_VPP

1230

change VPP_EN to SIO_SLP_S4#

change PWRGD_VPP to PWR_2D5V_PG

NEED EE CHECK

NEED EE CHECK

1230 change P_5V_A to 5V_S5

1230 change P_3.3V_A to 3D3V_S5

Design Current=0.7A

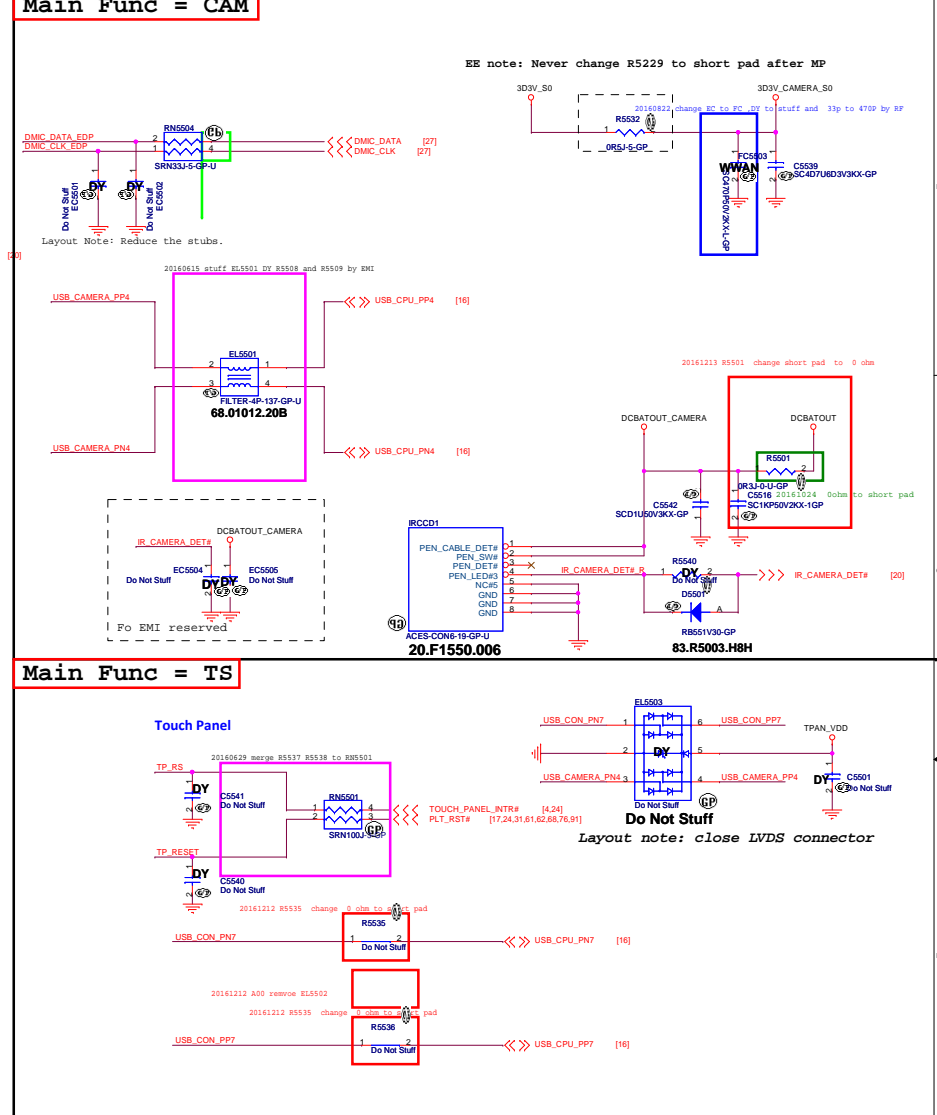
RT9025 for 1D8V_S5

Design Current = 454mA

$$V_{out} = 0.8V * (R1 + R2) / R2$$

2.DIS


	Main Func = CAM
--	-----------------



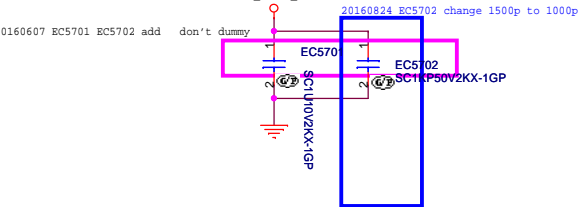
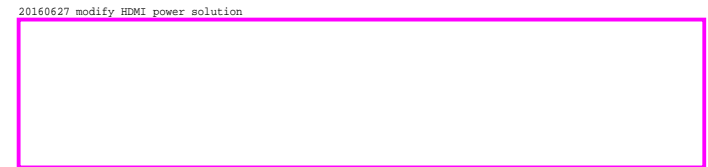
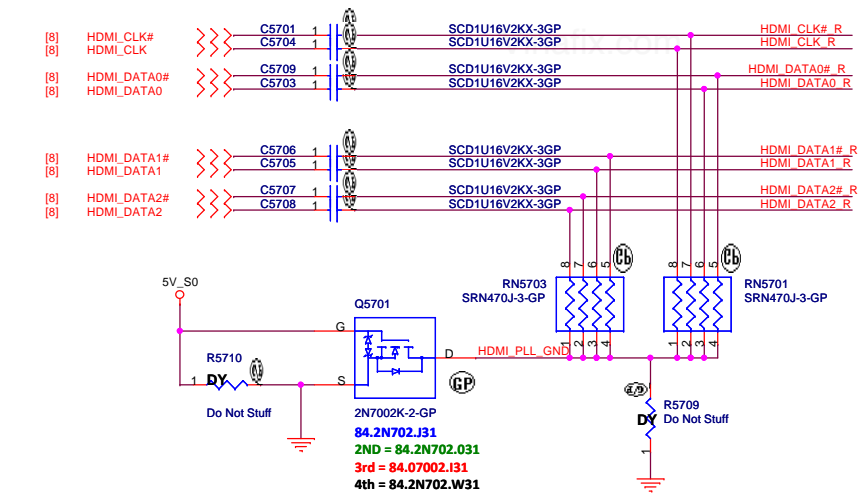
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2.DIS

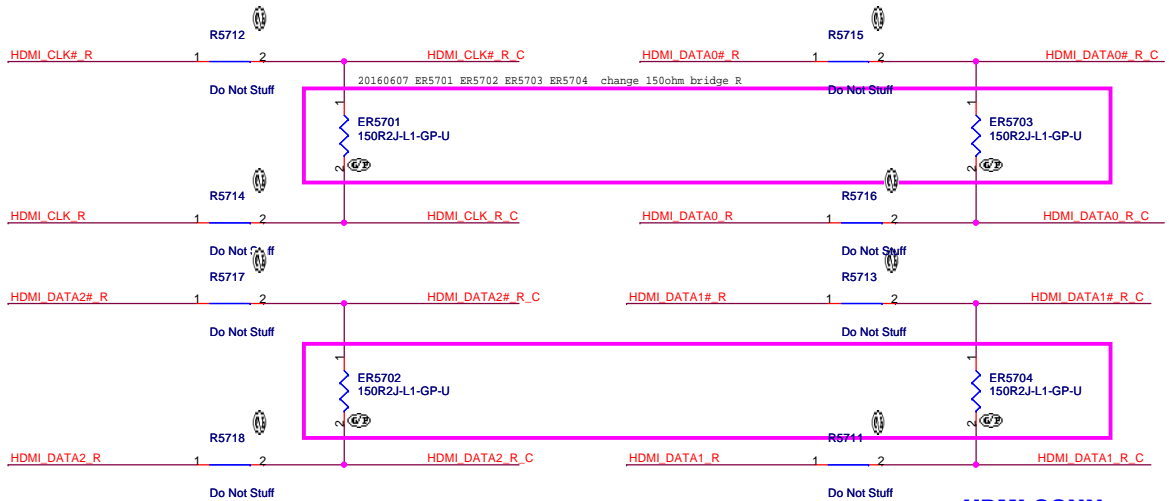
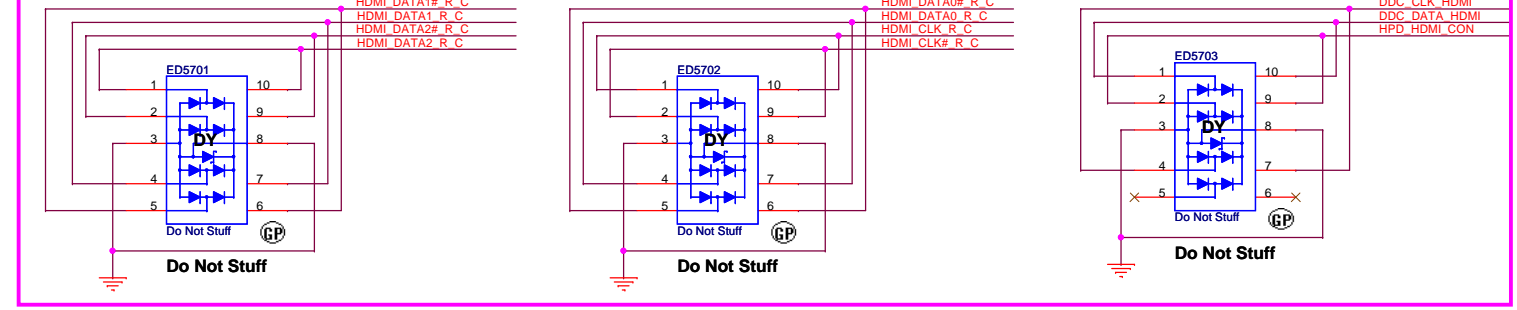
		Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title CRT			
Size A4	Document Number Taos KBL-U		Rev X00
Date: Monday, December 26, 2016		Sheet 56	of 105

Main Func = HDMI

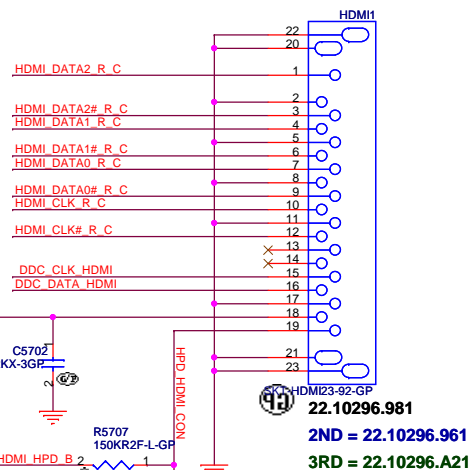


20160615 stuff by EMI
20160623 modify 75.00524.A73 to 75.08808.073
20161018 change stuff to DY by EMI

EMI Request:




HDMI CONN



Vinafix.com




2.DIS

		Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title (Reserved)			
Size A4	Document Number Taos KBL-U		Rev X00
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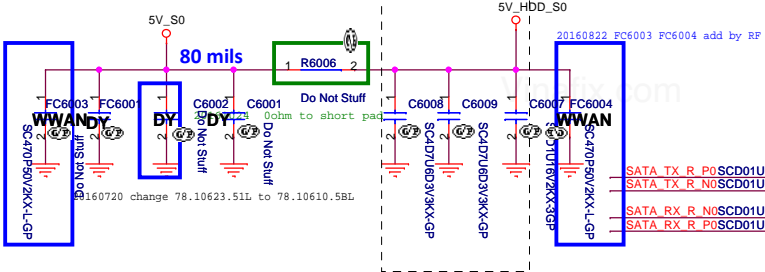
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2.DIS

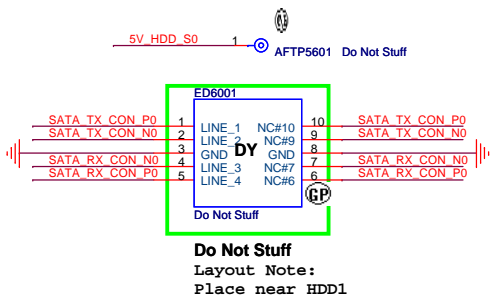
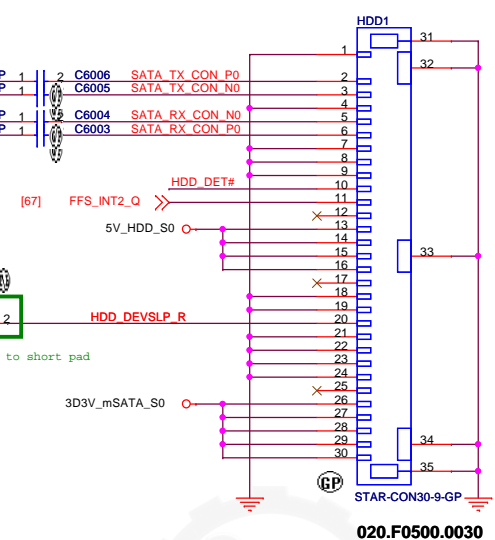
		Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title (Reserved)			
Size A4	Document Number Taos KBL-U		Rev X00
Date: Monday, December 26, 2016		Sheet 59 of	105

Main Func = HDD

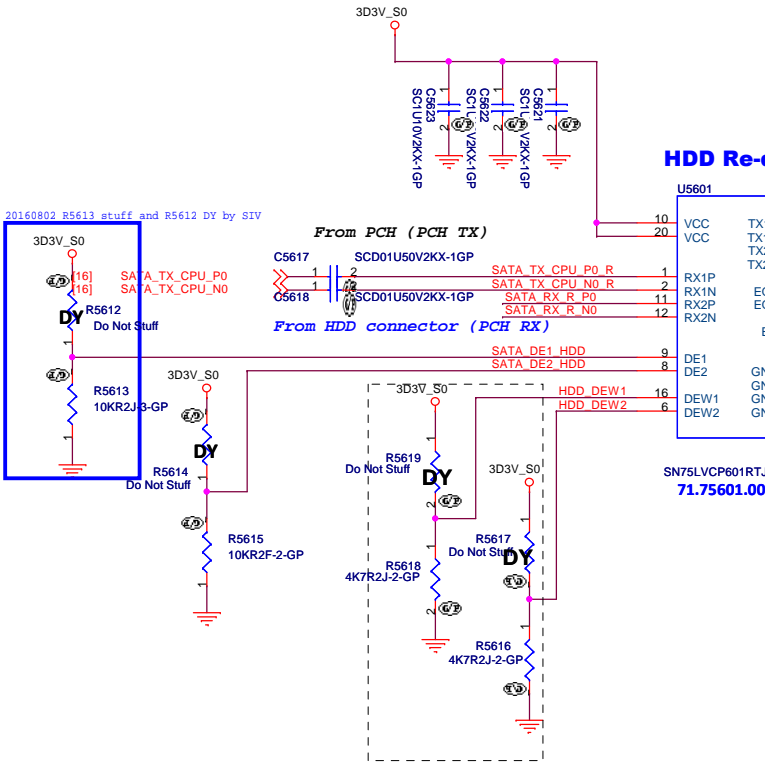
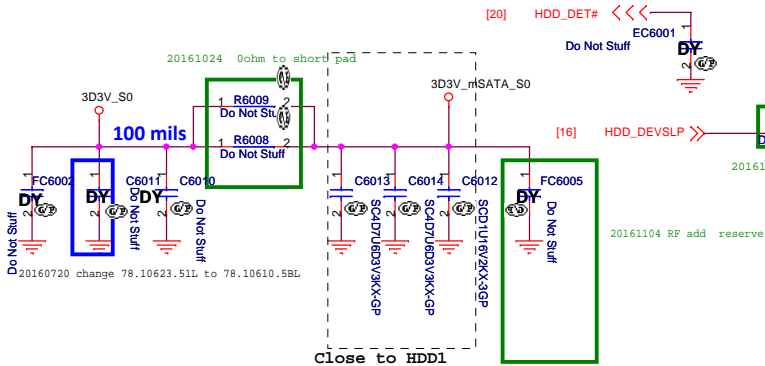
20160822 FC6003 FC6004 add by RF



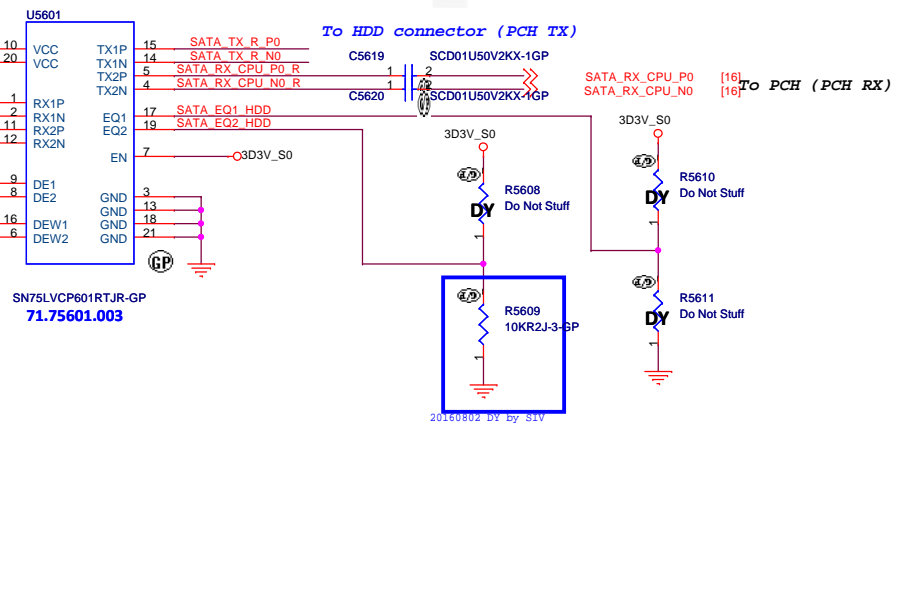
SATA HDD Connector



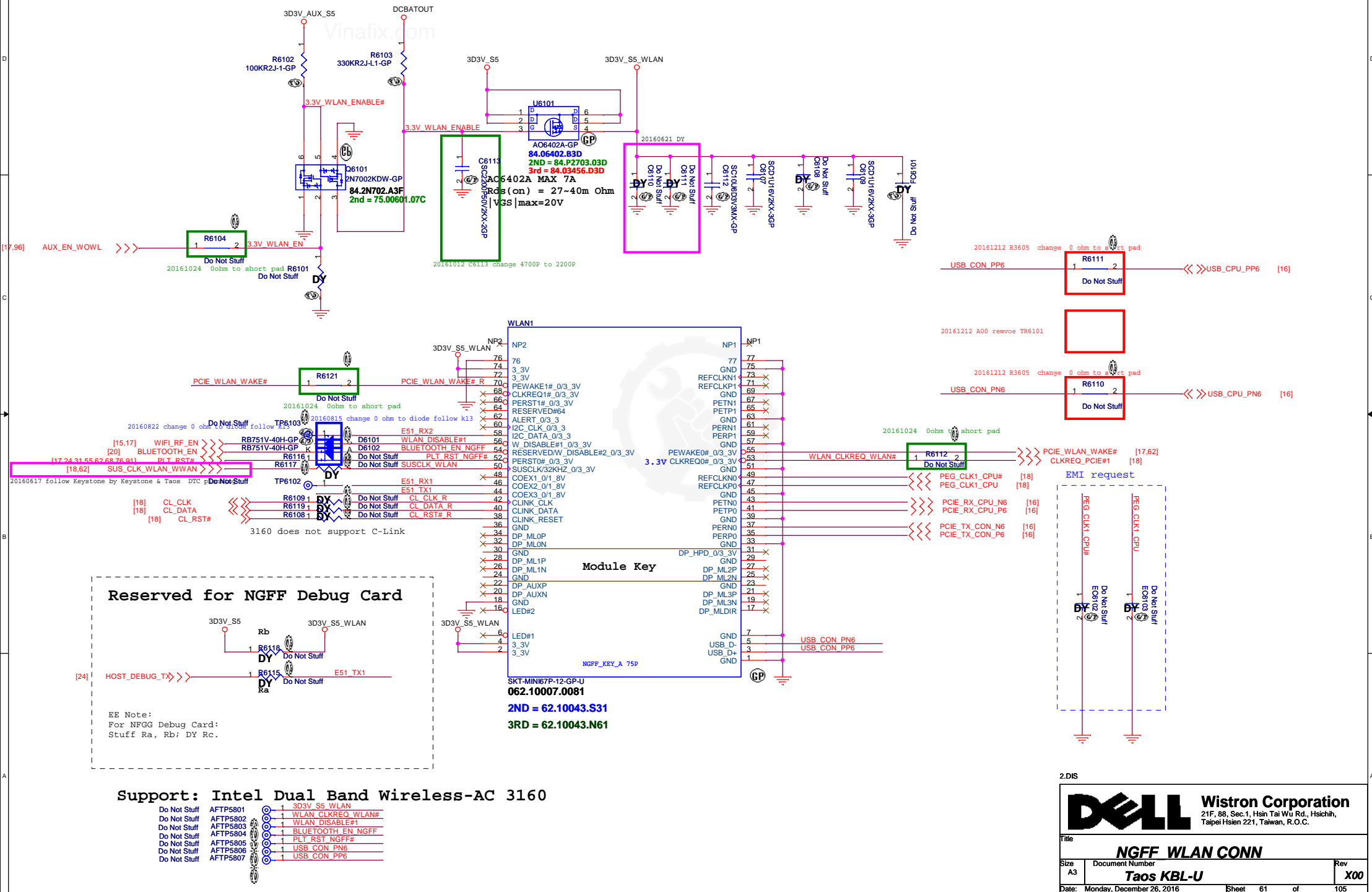
Do Not Stuff
Layout Note:
Place near HDD1



HDD Re-driver



Main Func = WLAN



2.DIS



Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

[illegible]**NGFF WLAN CONN**

Size

Document Number

Taos KBL-U

Date _____

Date: Monday, December 26, 2016

Shee

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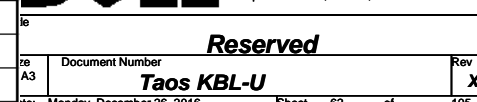
Rev

Yoo

XU

105

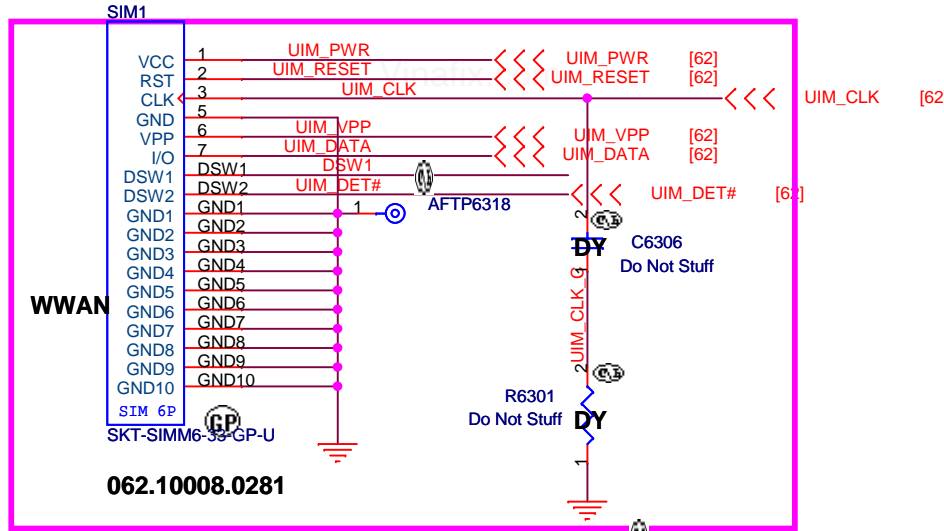
NGFF(WWAN/SSD)



STATE#	CONFIG_0	CONFIG_1	Module Type
0	GND	GND	SSD-SATA
8	NC	GND	WWAN
15	NC	NC	No Module Present

SSID =WIRELESS

20160527 modify connector

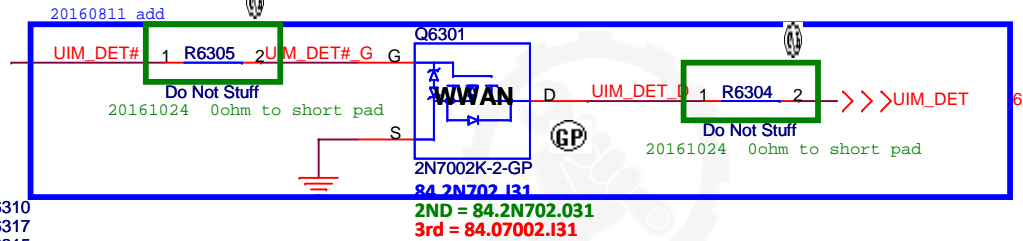
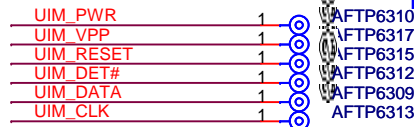


20160811 DY

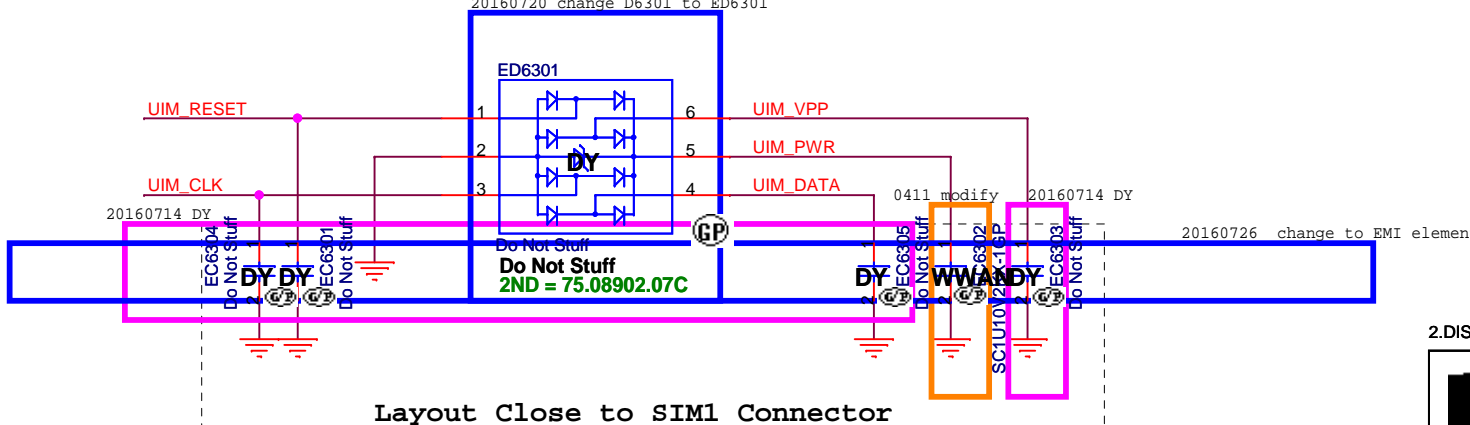


3D3V_S5_WWAN

PIN	62.10034.561 Micro SIM PinDefine
C1	VCC
C2	RST
C3	CLK
C4	Reserve
C5	GND
C6	VPP
C7	I/O
SW	SIM Card Detect
8	PTH GND
9	PTH GND
10	PTH GND
11	PTH GND



20160720 change D6301 to ED6301



2.DIS

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

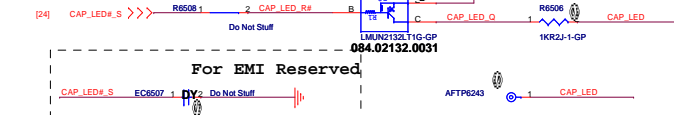
Title (Reserved)

Size A4	Document Number	Rev X00
Taos KBL-U		

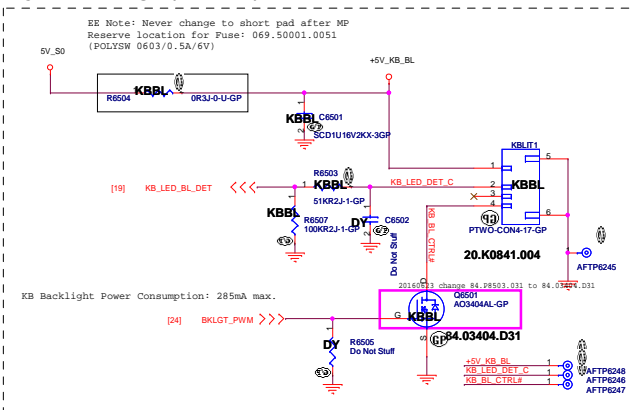
Date: Monday, December 26, 2016 Sheet 63 of 105

Main Func = KB					Main Func = TPAD				
----------------	--	--	--	--	------------------	--	--	--	--

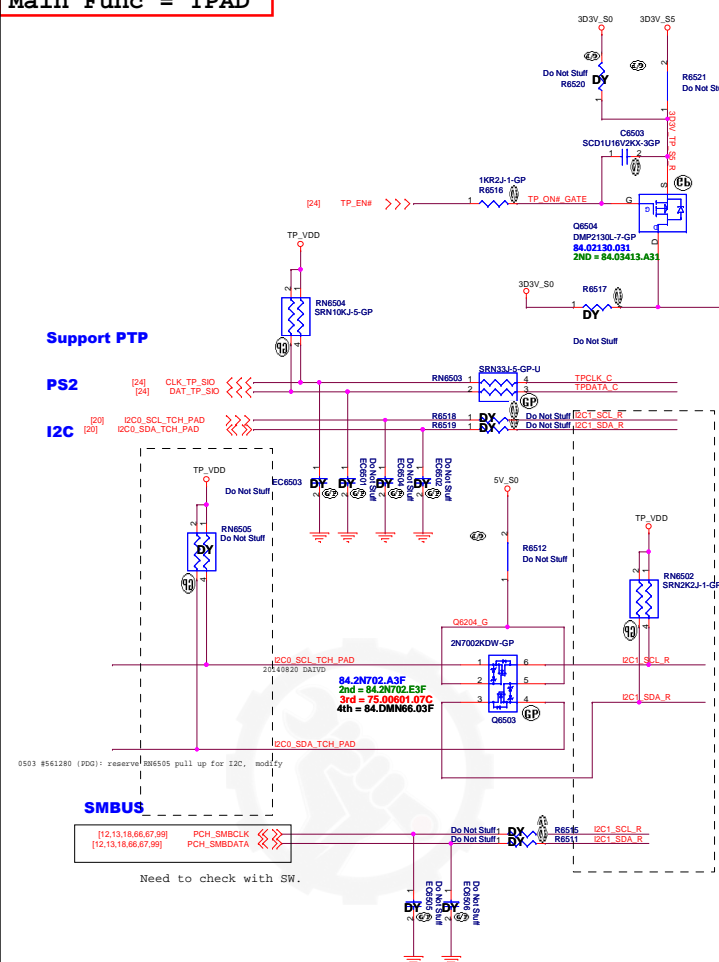
CAP LED Control
LOW actived from KBC GPIO



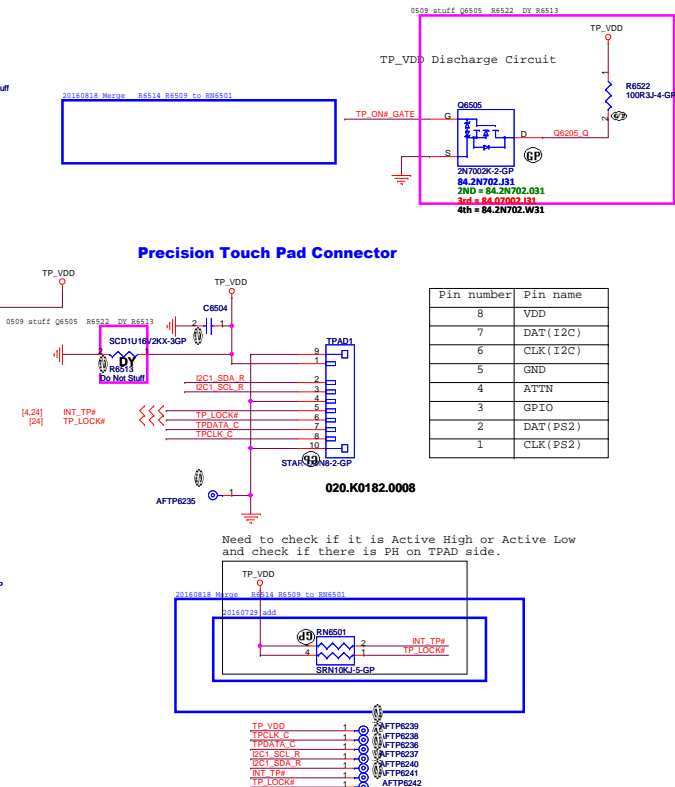
Keyboard Backlight (Reserved)



	Main Func = TPAD
--	------------------



Precision Touch Pad Connector



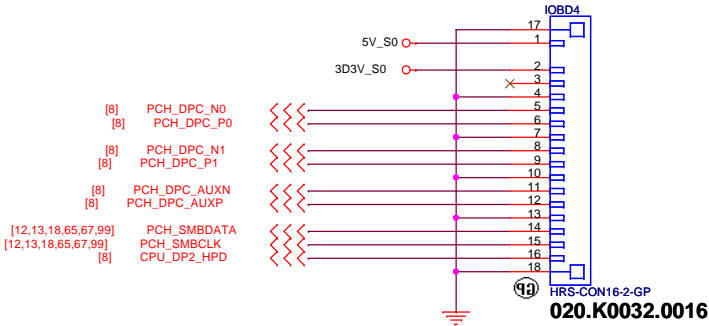
Pin number	Pin name
8	VDD
7	DAT(I2C)
6	CLK(I2C)
5	GND
4	ATTN
3	GPIO
2	DAT(PS2)
1	CLK(PS2)

Need to check if it is Active High or Active Low
and check if there is PH on TPAD side.

Main Func = IO Connector

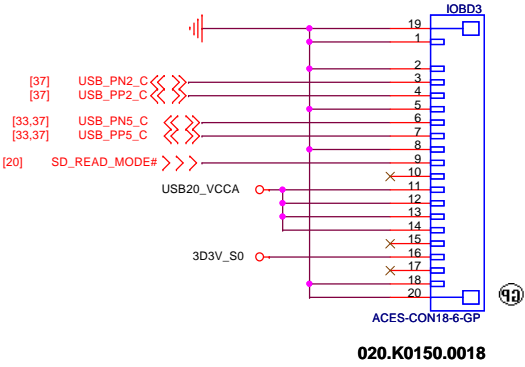
VGA Connector

Vinafix.com



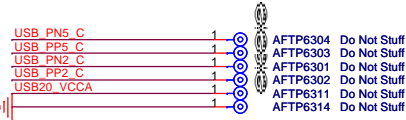
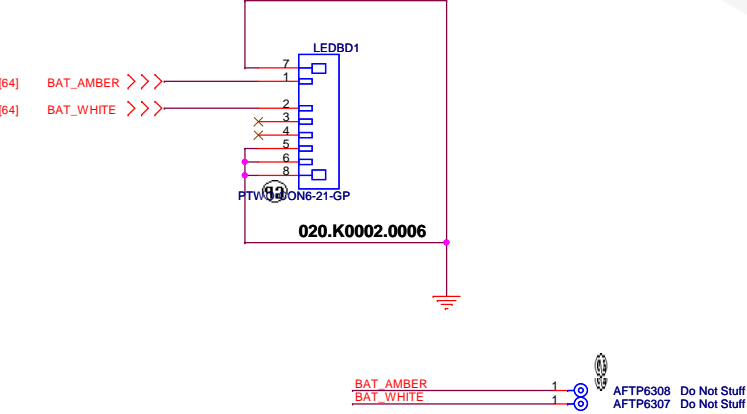
I/O Board Connector

USB3 (USB2.0)
Cardreader (USB2.0)



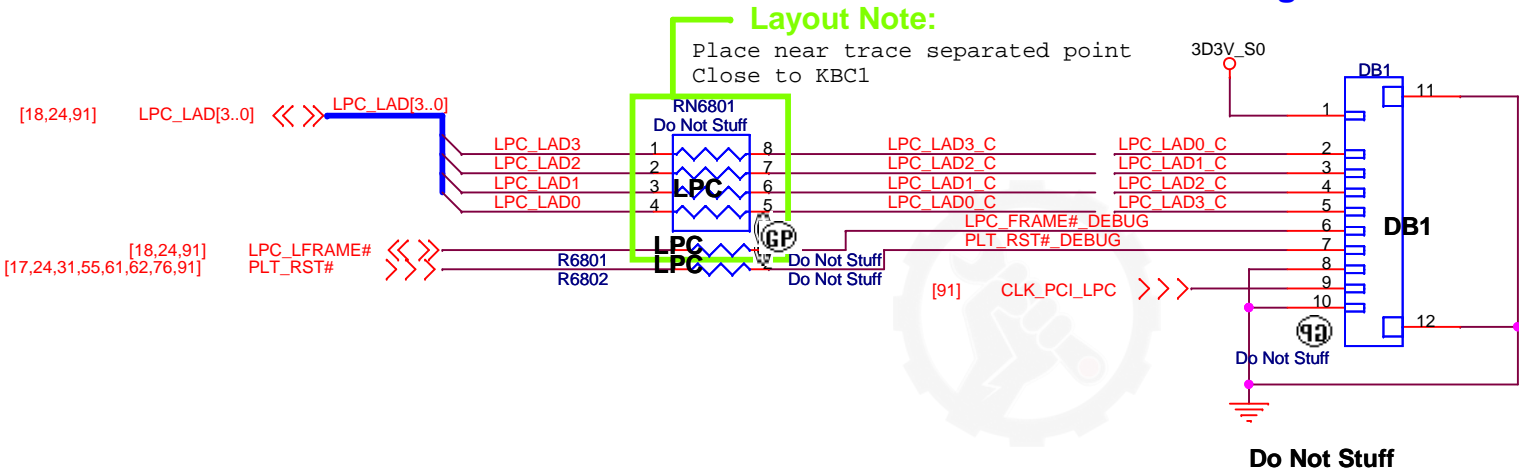
Pitch: 1mm
Power: 5 pins
GND: 5 pins

LED Connector




Main Func = Debug

Vinafix.com



20.D0075.110: Dummy Pad with solder mask is ZZ.00PAD.Y41
DB1 Optional: New one smaller LPC connector is 20.F1180.010.

2.DIS

		Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title Dubug connector			
Size A4	Document Number Taos KBL-U		Rev X00
Date: Monday, December 26, 2016		Sheet 68 of 105	

(Blanking)



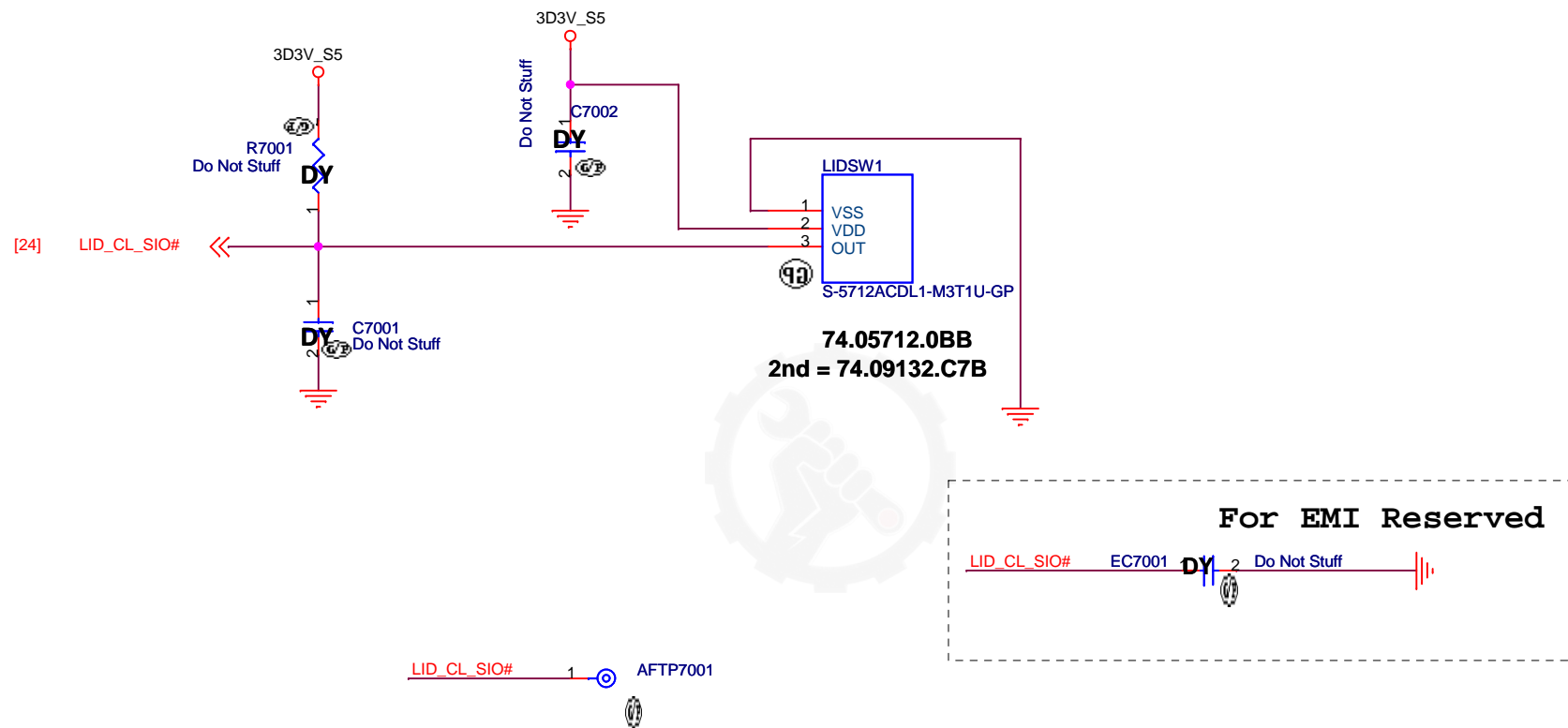
2.DIS

		Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title Reserved			
Size A4	Document Number Taos KBL-U		Rev X00
Date: Monday, December 26, 2016		Sheet 69 of	105


Main Func = Hall Sensor

Vinafix.com

LID sensoe




2.DIS

		Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title (Reserved)			
Size A4	Document Number Taos KBL-U		Rev X00
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(Blanking)



2.DIS


		Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title RESERVED			
Size A4	Document Number Taos KBL-U		Rev X00
Date: Monday, December 26, 2016		Sheet 71 of	105

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(Blanking)



2.DIS


		Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title			
USB3.0 PORT			
Size	Document Number		Rev
A4	Taos KBL-U		X00
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Main Func = dGPU

Vinafix.com




2.DIS

		Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title <i>Thunderbolt (3/5)(Reserved)</i>		
Size A4	Document Number Taos KBL-U	Rev X00
Date: Monday, December 26, 2016		Sheet 73 of 105

Vinafix.com



2.DIS

		Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title <i>Thunderbolt (4/5)(Reserved)</i>			
Size A4	Document Number Taos KBL-U		Rev X00
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2.DIS

		Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title <i>Thunderbolt (5/5)(Reserved)</i>			
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Main Func = dGPU

Vinafix.com

GFX & GPP, 85Ω
GFX & GPP CLK, 85Ω
GPU1A

1 OF 7

[16] PEG_TX_GPU_P0
[16] PEG_TX_GPU_N0
[16] PEG_TX_GPU_P1
[16] PEG_TX_GPU_N1
[16] PEG_TX_GPU_P2
[16] PEG_TX_GPU_N2
[16] PEG_TX_GPU_P3
[16] PEG_TX_GPU_N3

>>>
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AF30 PCIE_RX0P
AE31 PCIE_RX0N
AE29 PCIE_RX1P
AD28 PCIE_RX1N
AD30 PCIE_RX2P
AC31 PCIE_RX2N
AC29 PCIE_RX3P
AB28 PCIE_RX3N
AB30 PCIE_RX4P
AA31 PCIE_RX4N
AA29 PCIE_RX5P
Y28 PCIE_RX5N
Y30 PCIE_RX6P
W31 PCIE_RX6N
W29 PCIE_RX7P
V28 PCIE_RX7N
V30 NC#V30
U31 NC#U31
U29 NC#U29
T28 NC#T28
T30 NC#T30
R31 NC#R31
R29 NC#R29
P28 NC#P28
P30 NC#P30
N31 NC#N31
N29 NC#N29
M28 NC#M28
M30 NC#M30
L31 NC#L31
L29 NC#L29
K30 NC#K30

AH30 PEG_RX_GPU_P0
AG31 PEG_RX_GPU_N0
AG29 PEG_RX_GPU_P1
AF28 PEG_RX_GPU_N1
AF27 PEG_RX_GPU_P2
AF26 PEG_RX_GPU_N2
AD27 PEG_RX_GPU_P3
AD26 PEG_RX_GPU_N3
AC25
AB25
Y23
Y24
AB27
AB26
Y27
Y26
W24
W23
V27
U26
U24
U23
T26
T27
T24
T23
P27
P26
P24
P23
M27
M26

C7301 1
C7302 1
C7303 1
C7304 1
C7305 1
C7306 1
C7307 1
C7308 1

SCD22U10V2KX-1GP
SCD22U10V2KX-1GP
SCD22U10V2KX-1GP
SCD22U10V2KX-1GP
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SCD22U10V2KX-1GP
SCD22U10V2KX-1GP

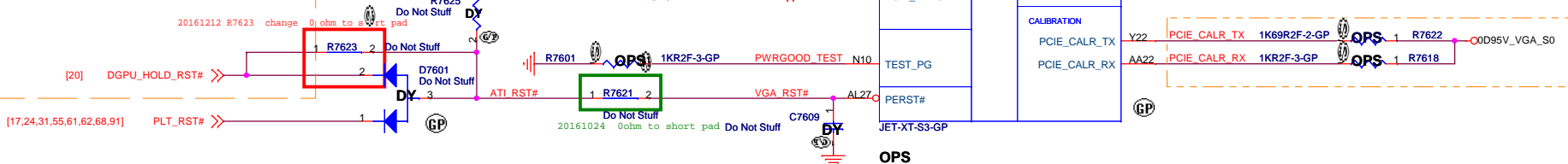
>>>
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>>>

[16] PEG_RX_CPU_P0
[16] PEG_RX_CPU_N0
[16] PEG_RX_CPU_P1
[16] PEG_RX_CPU_N1
[16] PEG_RX_CPU_P2
[16] PEG_RX_CPU_N2
[16] PEG_RX_CPU_P3
[16] PEG_RX_CPU_N3

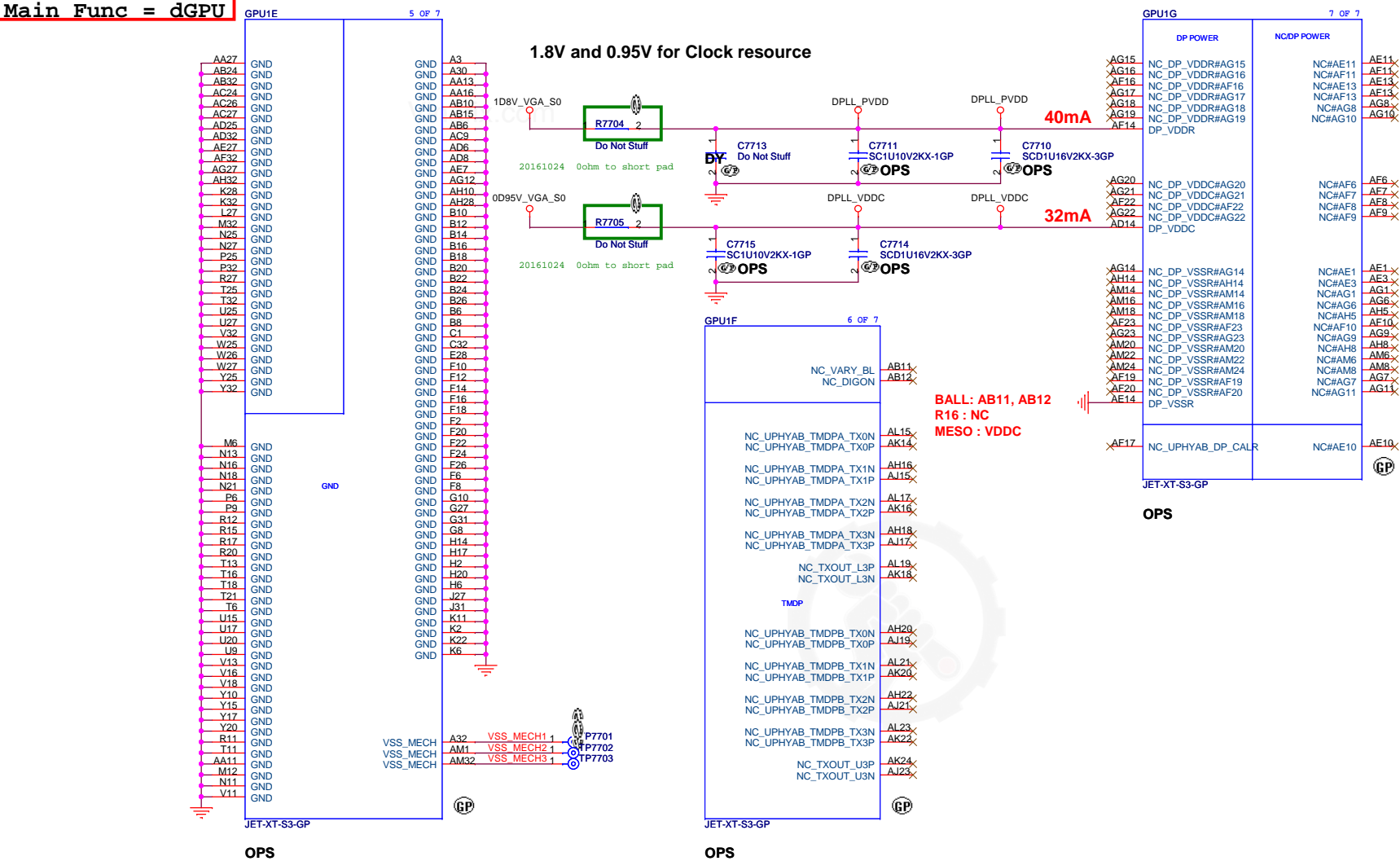
Table 3-5 PCI Express® Bus Interface

Pin Name	I/O	Description
PERSTb	I	Fundamental reset. 3.3-V tolerant pad. This signal must be asserted during any fundamental reset event, such as power up, warm boot, reset button pressed, CTL-ALT-DEL, Windows restart, or wake from D3.
PCIE_REFCLKP/N	I	PCI Express PLL differential reference clock (+/-). 100-MHz (± 300 ppm) input frequency; 0-V to 0.7-V single-ended swing.
PCIE_TX[7:0]P/N	O	PCI Express transmitter output data channel TX[7:0] (+/-). Differential serial data transmitted up to a 8.0-GT/s bit rate.
PCIE_RX[7:0]P/N	I	PCI Express receiver input data channel RX[7:0] (+/-). Differential serial data received up to a 8.0-GT/s bit rate.
PCIE_CALR_RX	I	Connect to PCIE_VDDC through a 1-kΩ (1% tolerance) resistor.
PCIE_CALR_TX	I	Connect to PCIE_VDDC through a 1.69-kΩ (1% tolerance) resistor.
CLKREQB	O	Reserved, do not connect on the PCB.

DGPU_HOLD_RST#	
H	dGPU mode
L	IGPU
H	IGPU with BACO



Main Func = dGPU



X00

Main Func = dGPU

Vinafix.com

Please MVREF drivers and Caps close to ASIC

DDR3/GDDR3 Memory Stuff Option(R16)

	GDDR5	GDDR3	DDR3
MVDDQ	1.5V	1D35V	1.5V
Ra	40.2R	40.2R	40.2R
Rb	100R	100R	100R

Place all these componets very close to GPU (within 25mm) and keep all componets close to each other
This basic topology should be used for DRAM_RST for DDR3/GDDR5

Main Func = dGPU

Vinafix.com

Please MVREF drivers and Caps close to ASIC

DDR3/GDDR3 Memory Stuff Option(R16)

	GDDR5	GDDR3	DDR3
MVDDQ	1.5V	1D35V	1.5V
Ra	40.2R	40.2R	40.2R
Rb	100R	100R	100R

Place all these componets very close to GPU (within 25mm) and keep all componets close to each other
This basic topology should be used for DRAM_RST for DDR3/GDDR5

Main Func = dGPU

Vinafix.com

Please MVREF drivers and Caps close to ASIC

DDR3/GDDR3 Memory Stuff Option(R16)

	GDDR5	GDDR3	DDR3
MVDDQ	1.5V	1D35V	1.5V
Ra	40.2R	40.2R	40.2R
Rb	100R	100R	100R

Place all these componets very close to GPU (within 25mm) and keep all componets close to each other
This basic topology should be used for DRAM_RST for DDR3/GDDR5

Jet Setting

Debug only, for clock observation, if not needed, DNI

GPU1C

3 OF 7

MEMORY INTERFACE

ADD

DM

DQS

Ctrl

CLK

CMD

Ctrl, CS

Ctrl

CMD

2.DIS

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File **GPU (3/5) VRAM I/F**

Size A3 Document Number **Taos KBL-U** Rev **X00**

Date: Monday, December 26, 2016 Sheet 78 of 105

Main Func = dGPU

Vinafix.com

Please MVREF drivers and Caps close to ASIC

DDR3/GDDR3 Memory Stuff Option(R16)

	GDDR5	GDDR3	DDR3
MVDDQ	1.5V	1D35V	1.5V
Ra	40.2R	40.2R	40.2R
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Place all these componets very close to GPU (within 25mm) and keep all componets close to each other
This basic topology should be used for DRAM_RST for DDR3/GDDR5

Jet Setting

Debug only, for clock observation, if not needed, DNI

GPU1C

3 OF 7

MEMORY INTERFACE

ADD

DM

DQS

Ctrl

CLK

CMD

Ctrl, CS

Ctrl

CMD

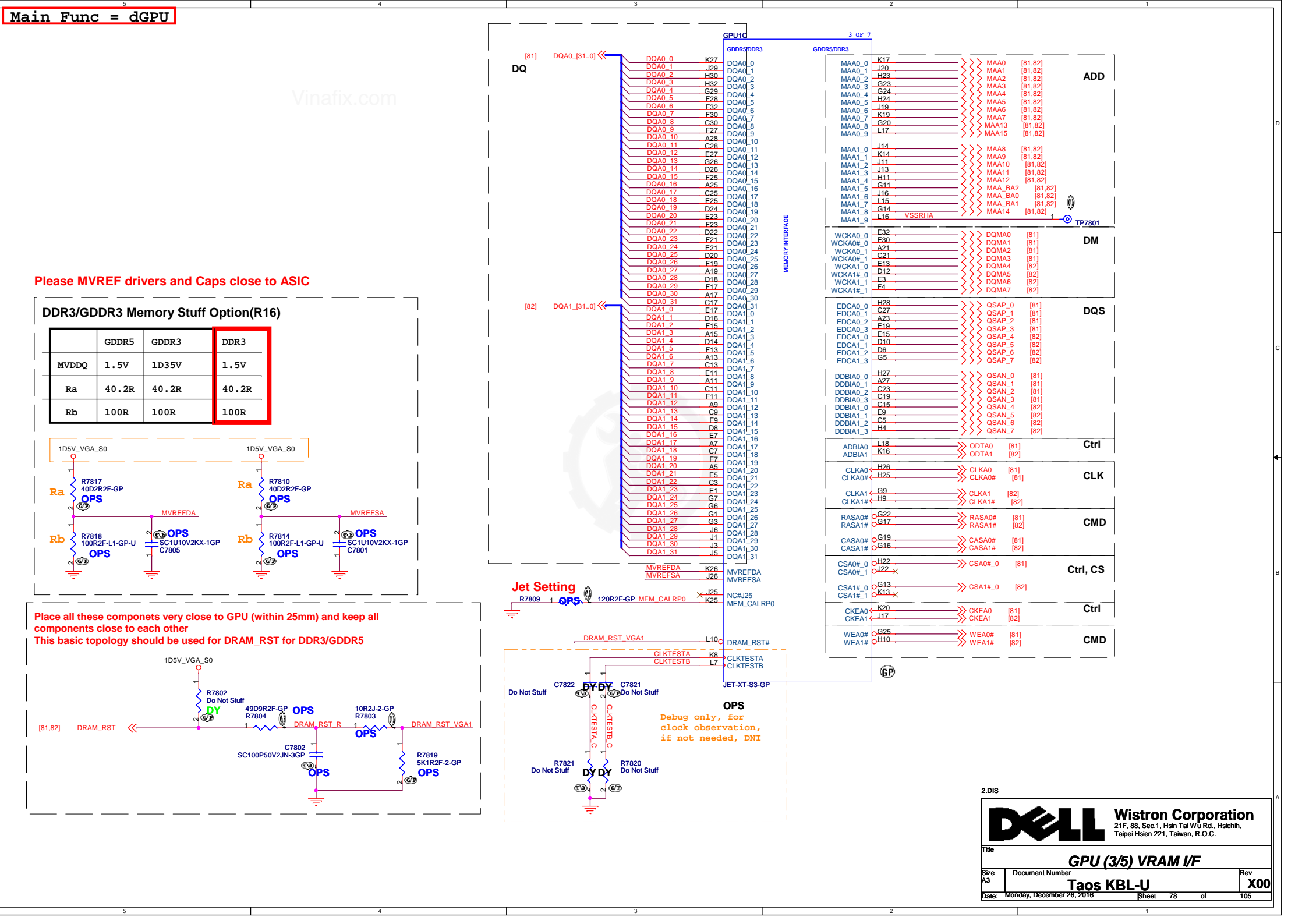
2.DIS

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File **GPU (3/5) VRAM I/F**

Size A3 Document Number **Taos KBL-U** Rev **X00**

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Main Func = dGPU

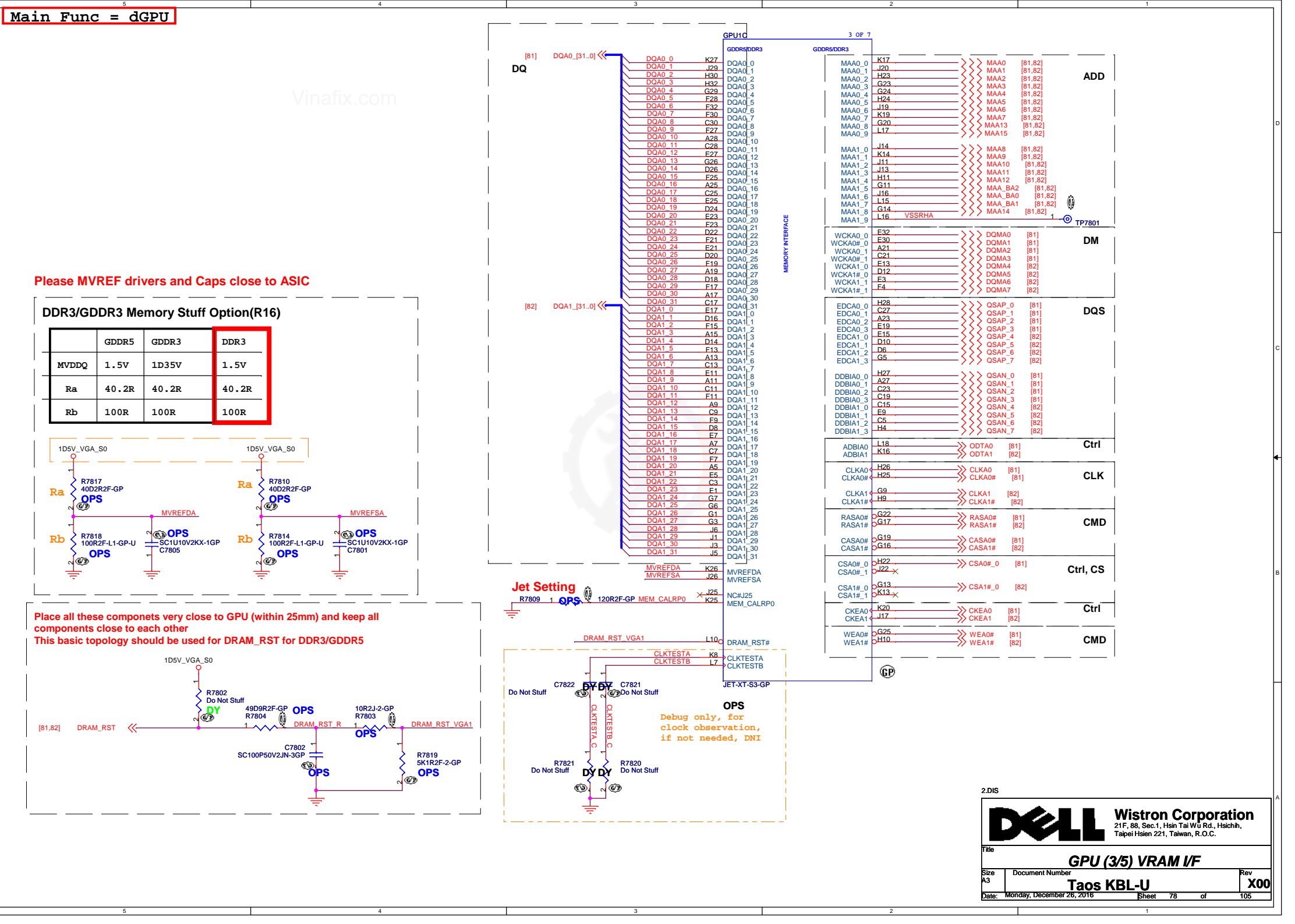
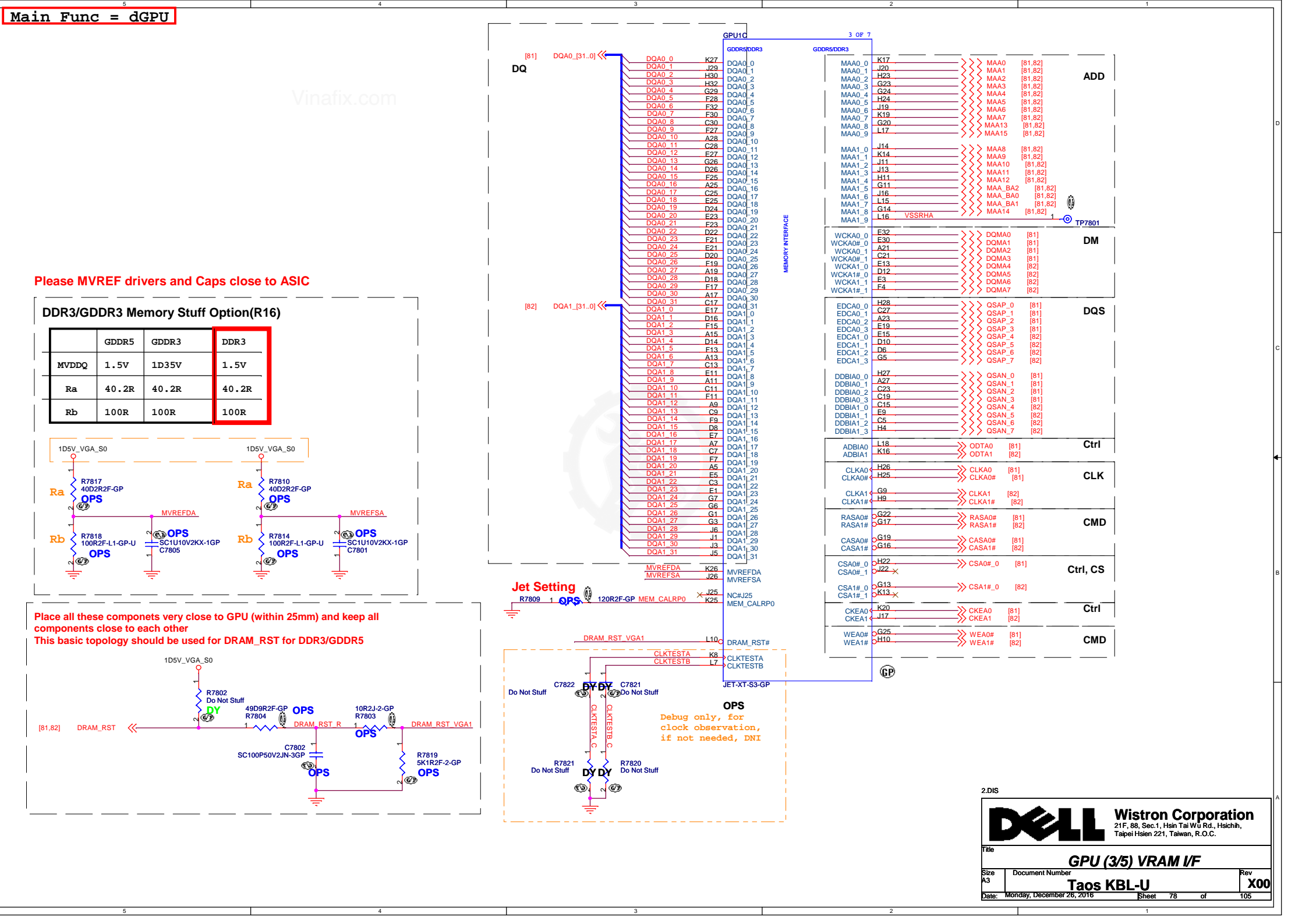
Vinafix.com

Please MVREF drivers and Caps close to ASIC

DDR3/GDDR3 Memory Stuff Option(R16)

	GDDR5	GDDR3	DDR3
MVDDQ	1.5V	1D35V	1.5V
Ra	40.2R	40.2R	40.2R
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Place all these componets very close to GPU (within 25mm) and keep all componets close to each other
This basic topology should be used for DRAM_RST for DDR3/GDDR5



Main Func = dGPU

Vinafix.com

Please MVREF drivers and Caps close to ASIC

DDR3/GDDR3 Memory Stuff Option(R16)

	GDDR5	GDDR3	DDR3
MVDDQ	1.5V	1D35V	1.5V
Ra	40.2R	40.2R	40.2R
Rb	100R	100R	100R

Place all these componets very close to GPU (within 25mm) and keep all componets close to each other
This basic topology should be used for DRAM_RST for DDR3/GDDR5

Jet Setting

Debug only, for clock observation, if not needed, DNI

GPU1C

3 OF 7

3 OF 7

ADD

DM

DQS

Ctrl

CLK

CMD

Ctrl, CS

Ctrl

CMD

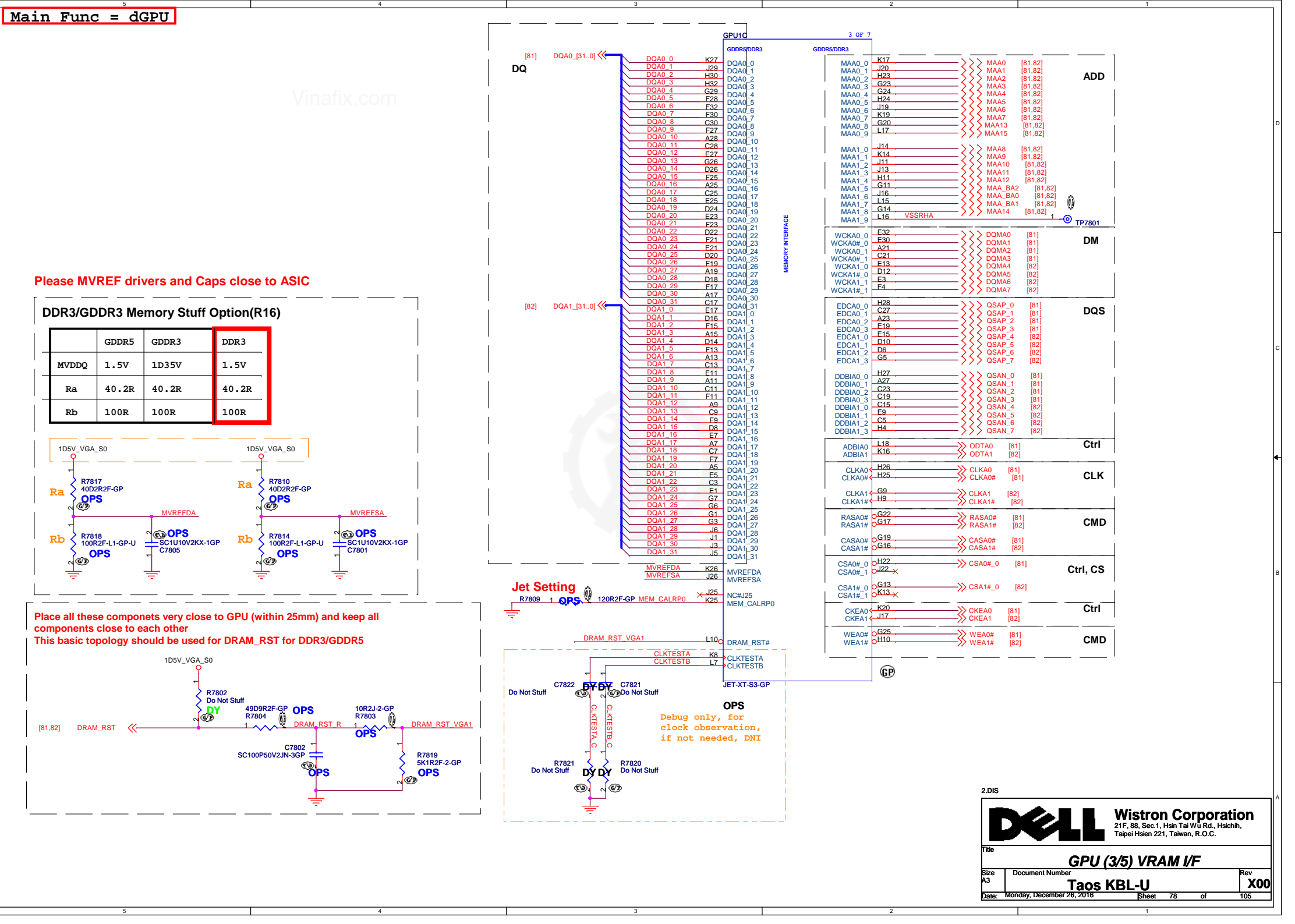
2.DIS

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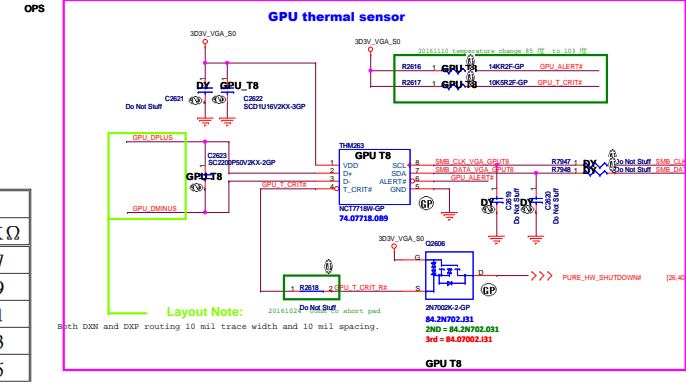
File **GPU (3/5) VRAM I/F**

Size A3 Document Number **Taos KBL-U** Rev **X00**

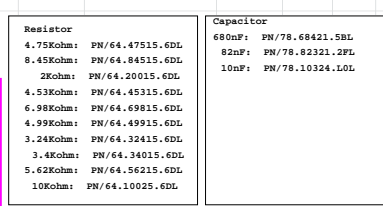
Date: Monday, December 26, 2016 Sheet 78 of 105



TEMPERATURE(°C)		T_CRIT#				
		2K Ω	7.5K Ω	10.5K Ω	14K Ω	18.7K Ω
ALERT#	2K Ω	77	87	97	107	117
	7.5K Ω	79	89	99	109	119
	10.5K Ω	81	91	101	111	121
	14K Ω	83	93	103	113	123
	18.7K Ω	85	95	105	115	125



D setting:								R_ave	R_std
Q2-Q1	Memory Type	Configuration	Row x Col x Bank bits	Channel Size	Vendor P/N	SMT quantity			
0:0									
000	Samsung - DDR3L	256M x 16		2GB	IC4W4G1646E-BC1A	4 pcs	30C	4750	
001	Micron - DDR3L	256M x 16		2GB	MT41J256M16L-Y-0910-N	4 pcs	8450	2000	
010	SK hynix - DDR3L	256M x 16		2GB	H5TC436E39R-ND	4 pcs	4530	2000	
011									
000									
001									
010									
011									



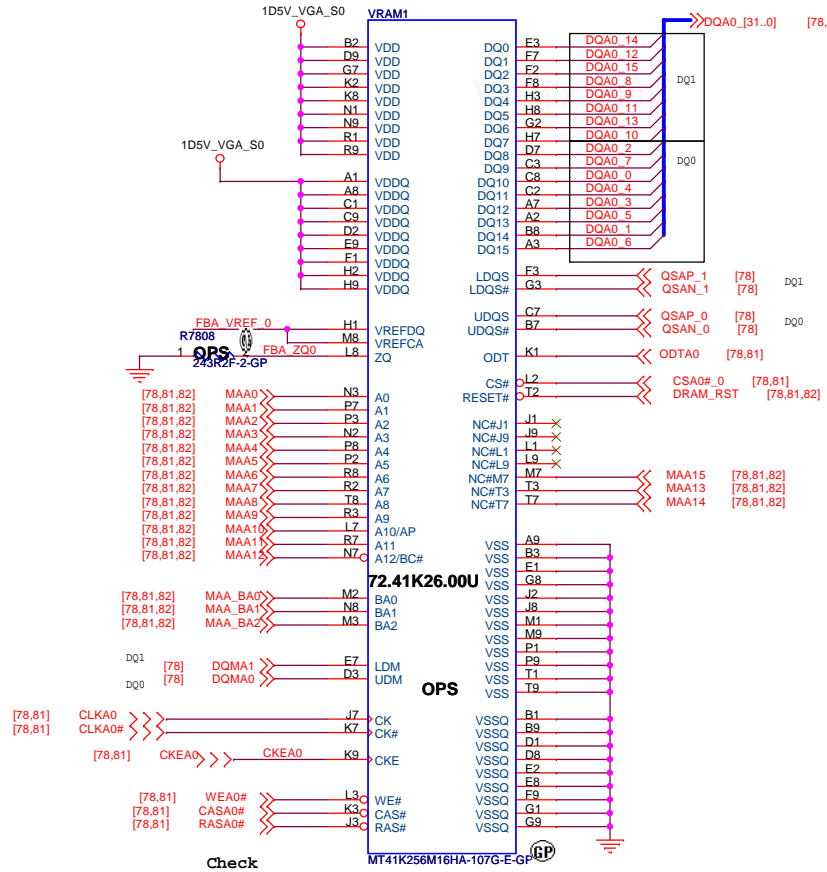
20160701 decap follow decap plan file



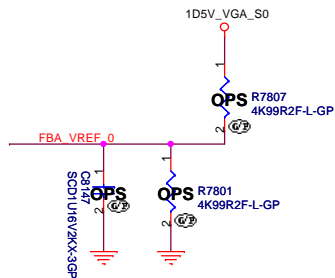
Main Func = dGPU

20160701 decap follow decap plan file

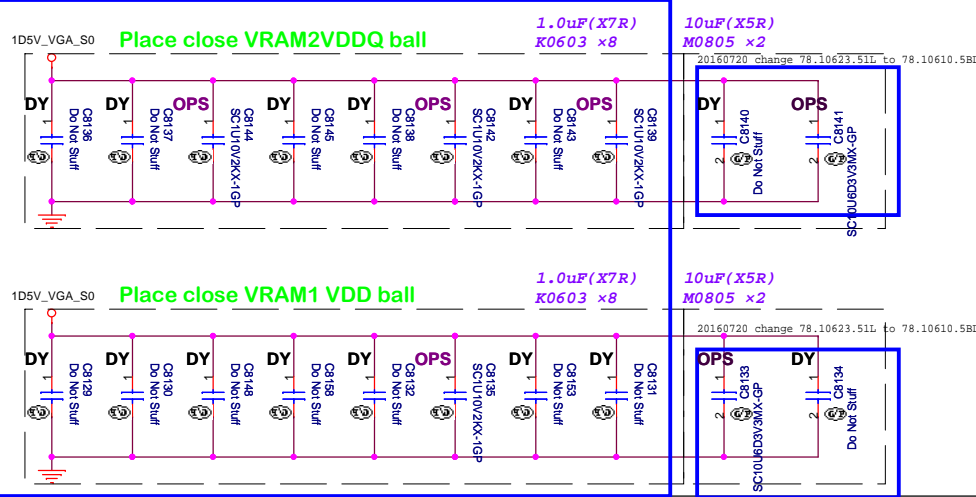
Data Bits 31:0 RANK 0



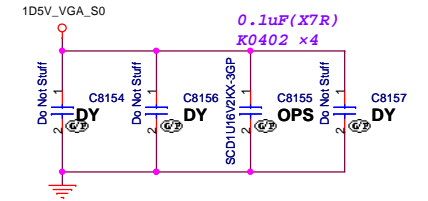
Frame Buffer Partition A-Lower Half



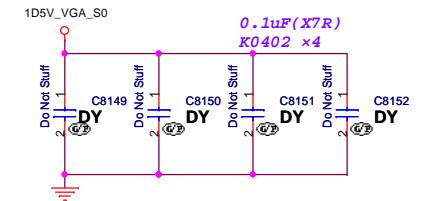
20160728 CAP change 78.10520.2BL to 78.10523.L2L



Place close VRAM2 VDD ball

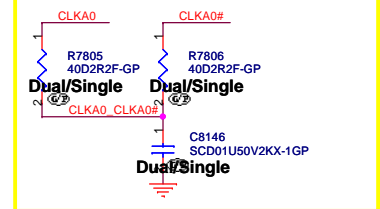


Place close VRAM1VDDQ ball



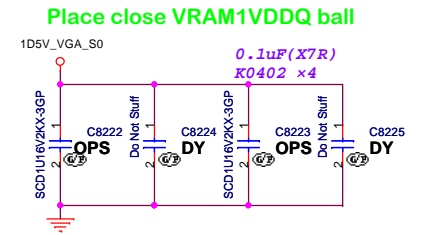
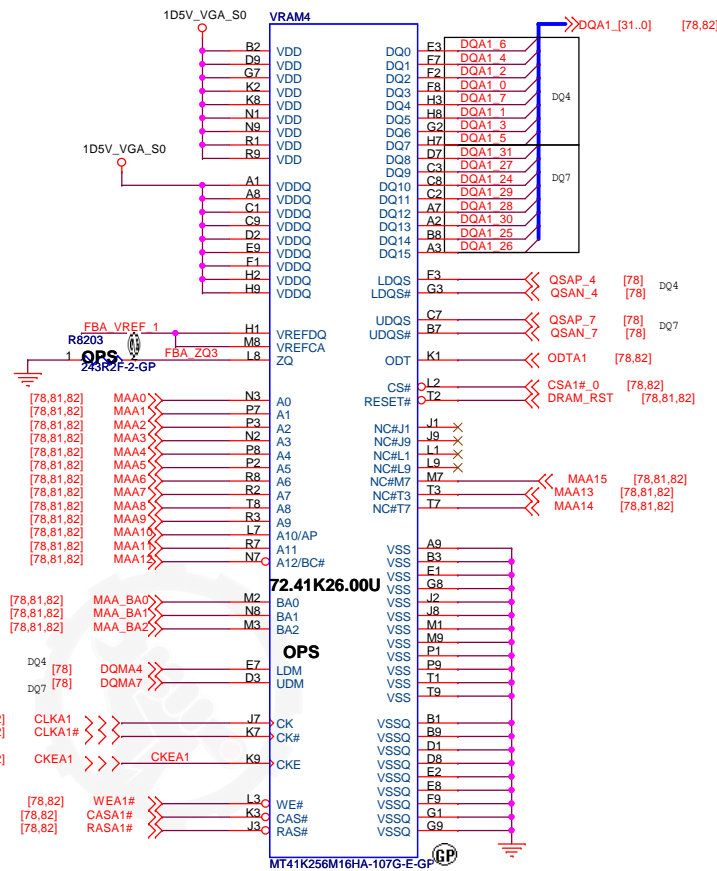
R7805 R7810

Single Rank, 40.2 Ohm = 64.40R25.6DL
Dual Rank, 80.6 Ohm = 64.80R65.6DL



2.DIS

Data Bits 63:32 RANK 0

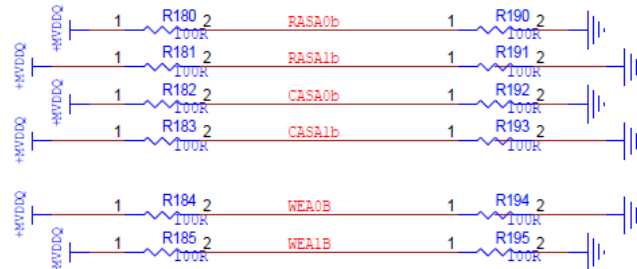
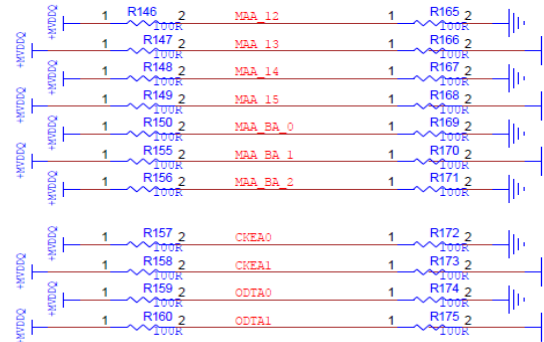
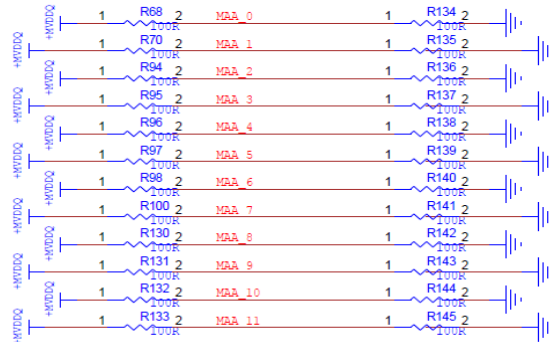
[illegible]

The diagram shows two identical circuit configurations. On the left, a resistor labeled R6201 4002R2F-GP is connected between the CLK_A1 signal line and ground. On the right, a resistor labeled R6202 4002R2F-GP is connected between the CLK_A1# signal line and ground. Both resistors are marked with a ground symbol, indicating they are pull-down resistors. The signals CLK_A1 and CLK_A1# are shown as input lines with a ground symbol next to them, indicating they are also pulled down.

Note : Dual Rank need add

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For DUAL RANK configuration,
termination might be required based on simulation results
the actual termination value should be OPTIMIZED by the simulation



2.DIS



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Title

(Reserved) VRAM5,6 (3/4)

Size

Document Number

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5 4 3 2 1


Main Func = dGPU

Data Bits 63:32 RANK 1

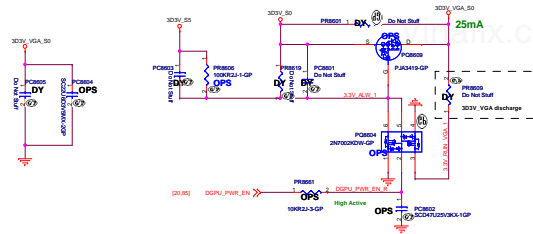
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2.DIS

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Title (Reserved) VRAM7,8 (4/4)		
Size A4	Document Number Taos KBL-U	Rev X00
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3D3V_S0 to 3D3V_VGA_S0 Transfer



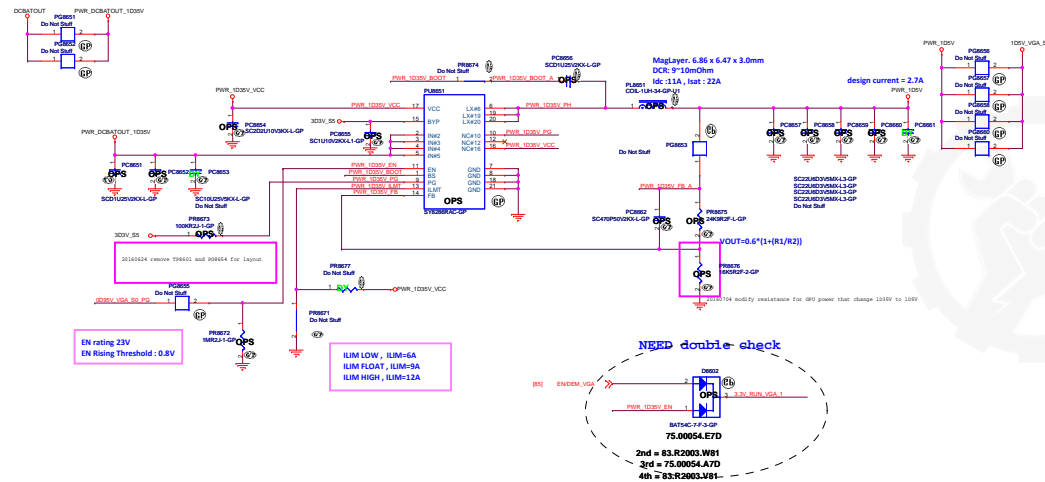
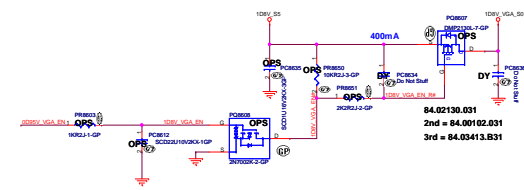
GPU PWR Sequencing

```
3D3V_VGAS0
=> 0D95V_VGA_S0/1D8V_VGA_S0
    => 1D35V_VGA_S0
        => VGA_CORE
```

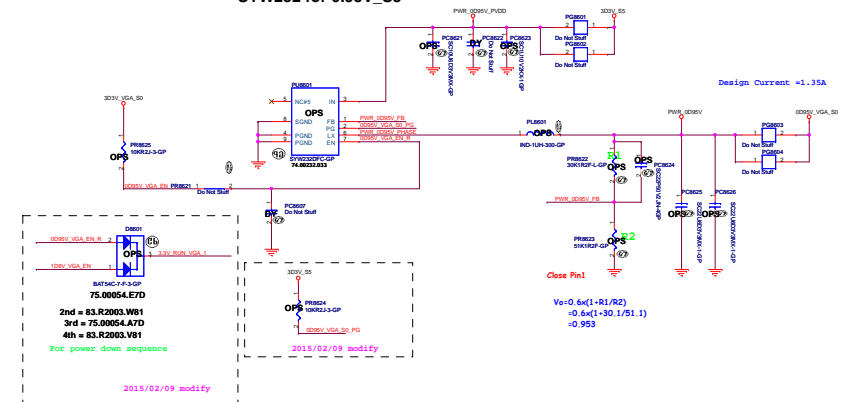
All the ASIC supplies must reach their respective nominal voltages withing **20ms** of the start of the ramp-up sequence, though a shorter ramp-up duration is preferred. The maximum slew rate on all rails is 50mV/us.

It is recommended that the 3.3V rail ramp up first.

It is recommended that the 0.95V rail reach at least 90% of its normal value no later than 2ms from the start of VDDC ramping up.



SYW232 for 0.95V_S5



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Title

Reserved

Size
A4

Document Number

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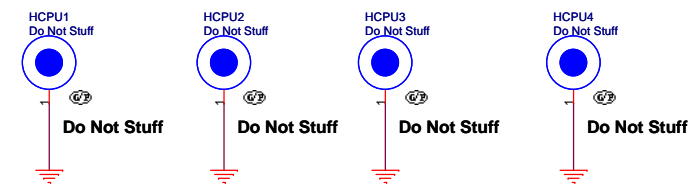
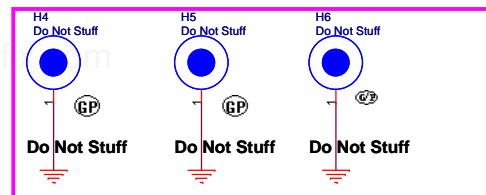
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Title			
<i>Reserved</i>			
Size A4	Document Number <i>Taos KBL-U</i>		Rev <i>X00</i>
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Main Func = UnusedParts



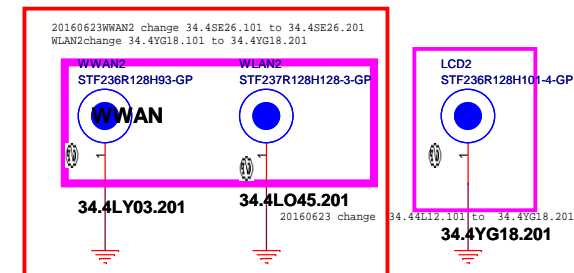
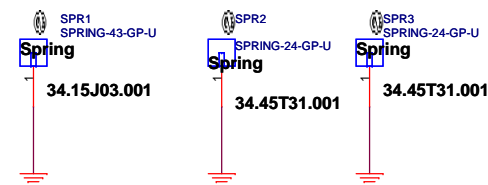
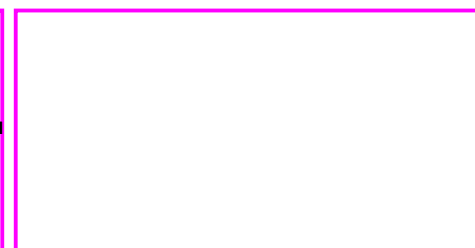
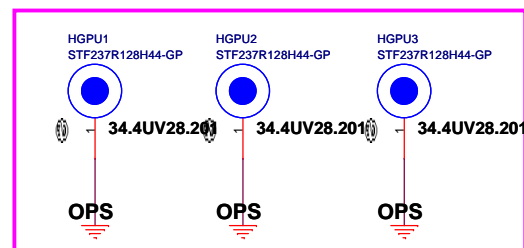
20160614 change by connector list



20161215 WWAN2 change 34.4SE26.201 to 34.4LY03.201 !! WLAN2 change 34.4YG18.201 to 34.4LO45.201

20160614 change by connector list

20160711 remove HGPU4 HGPU5 HGPU6

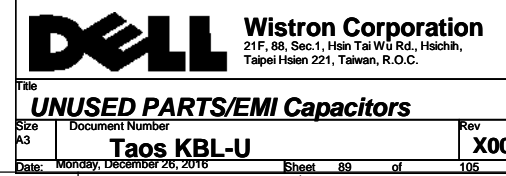
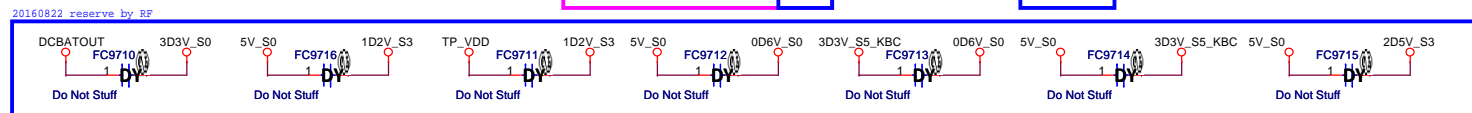
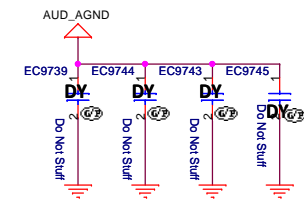
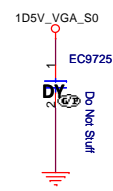
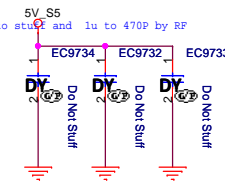
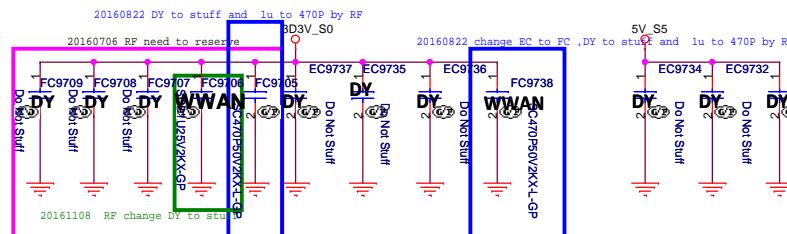
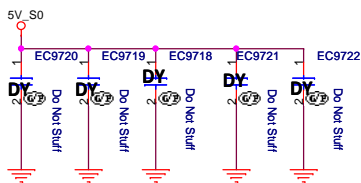
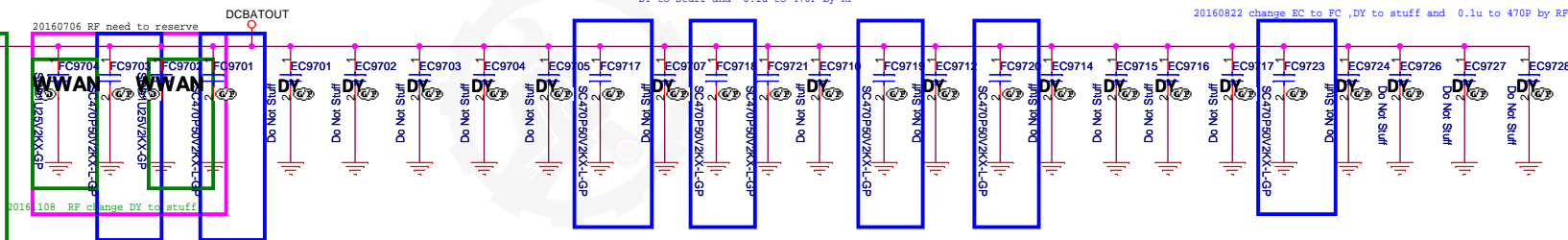
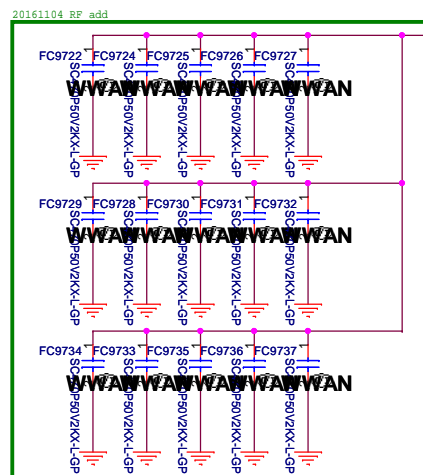


Main Func = EMICapacitors

Mind the voltage rating of the caps.


20160822 change EC9706 EC9708 EC9711 EC9713 EC9709
to FC9717 FC9718 FC9719 FC9720 FC9721 ,
DY to stuff and 0.1u to 470P by RF

20160822 change EC to FC ,DY to stuff and 0.1u to 470P by RF



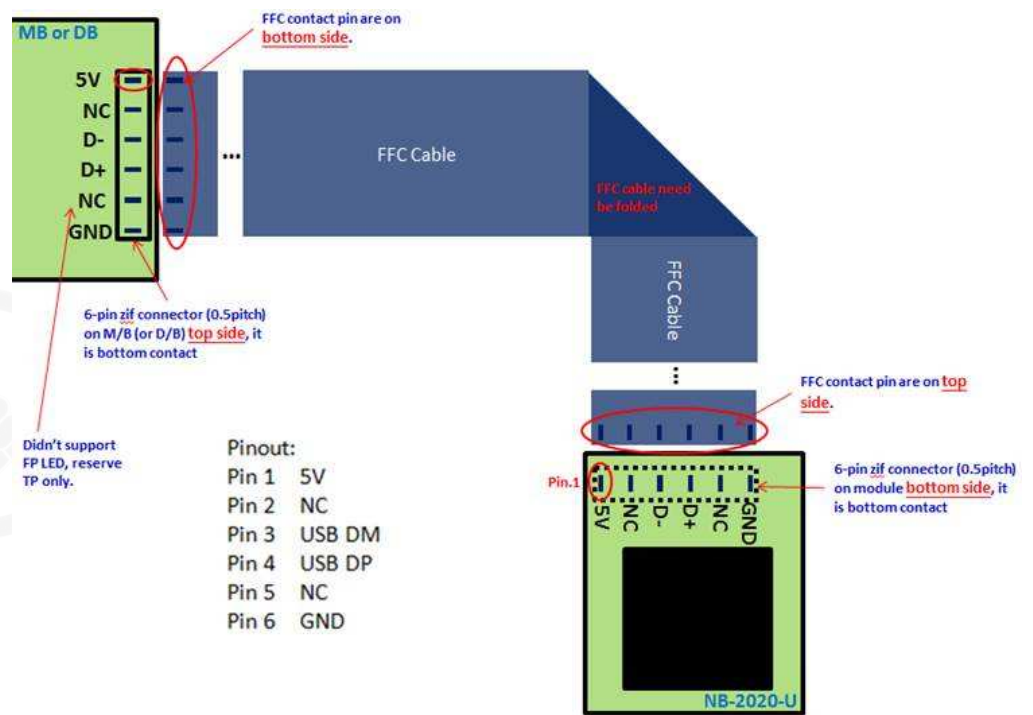
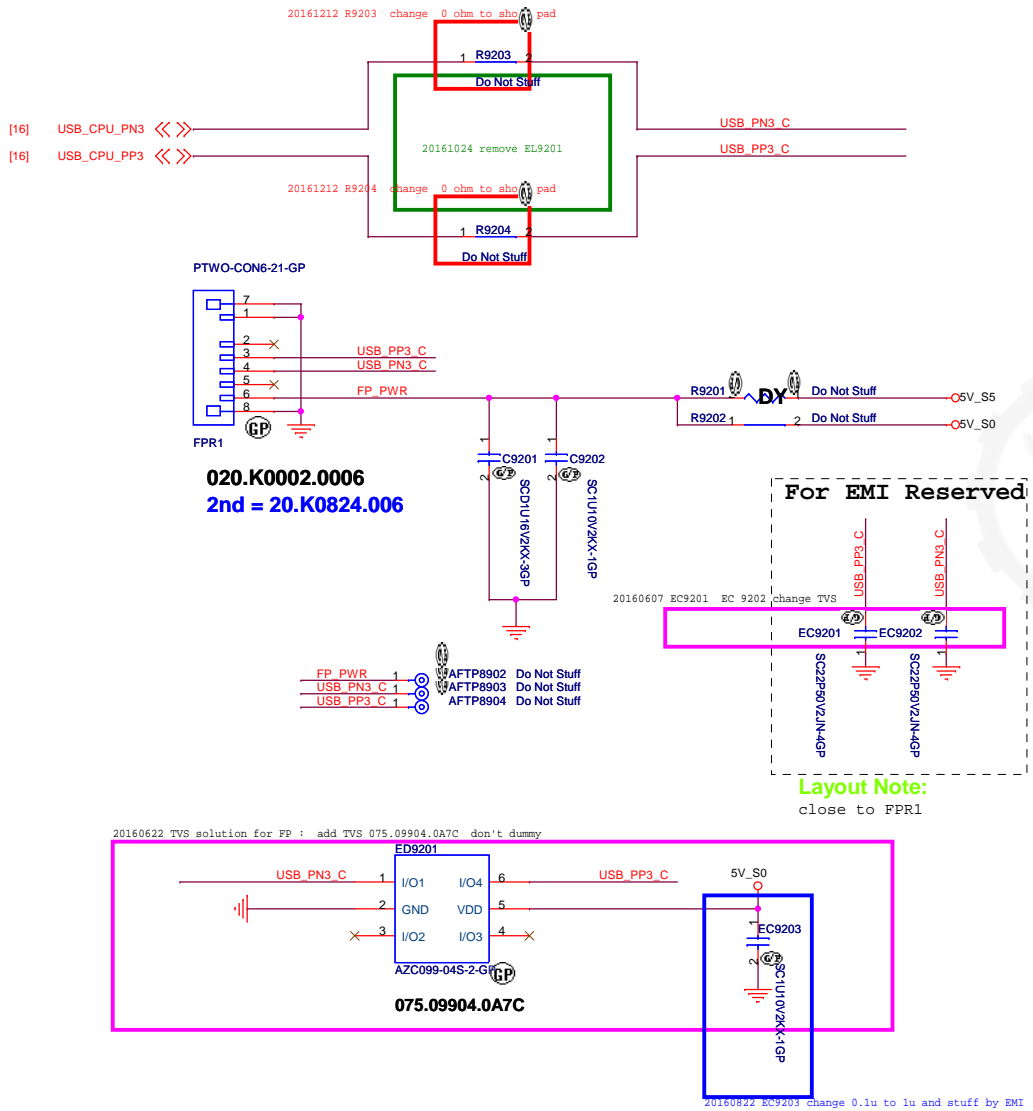
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SSID = Finger Print


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Size A4	Document Number Taos KBL-U		Rev X00
Date: Monday, December 26, 2016		Sheet 93 of	105

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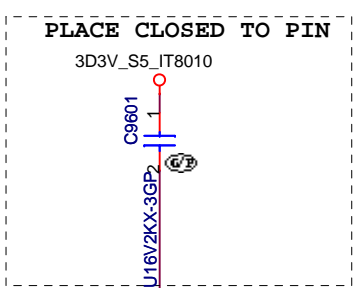
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Title (Reserved)			
Size A4	Document Number Taos KBL-U		Rev X00
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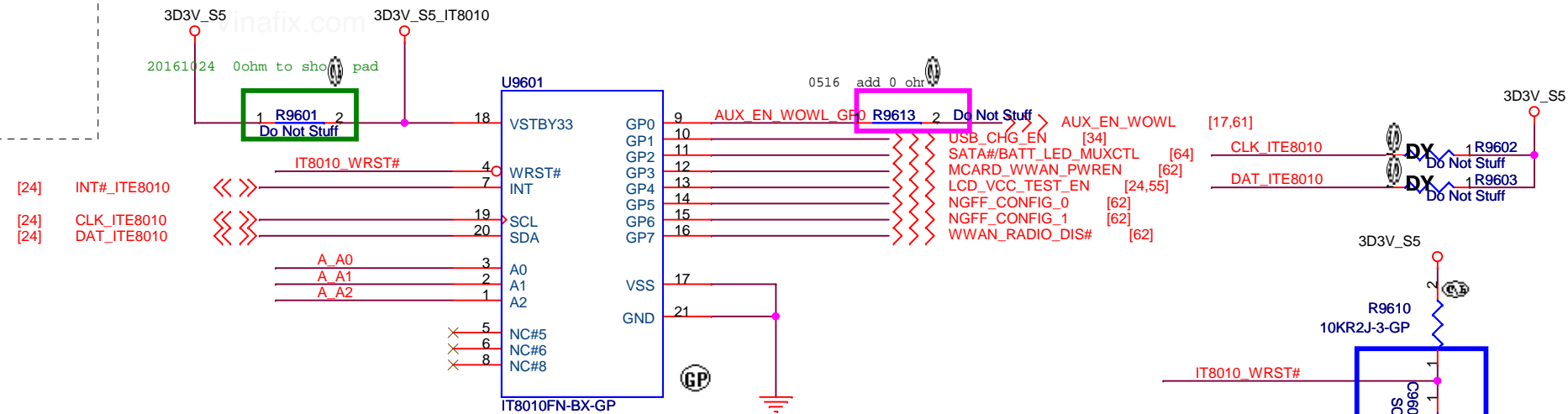


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All I/O Signals are 3.3V CMOS Level

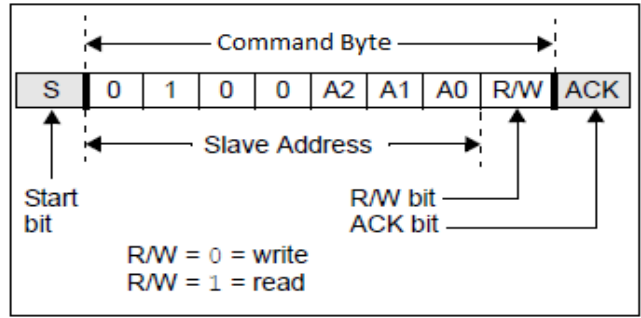
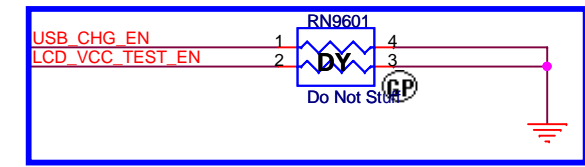
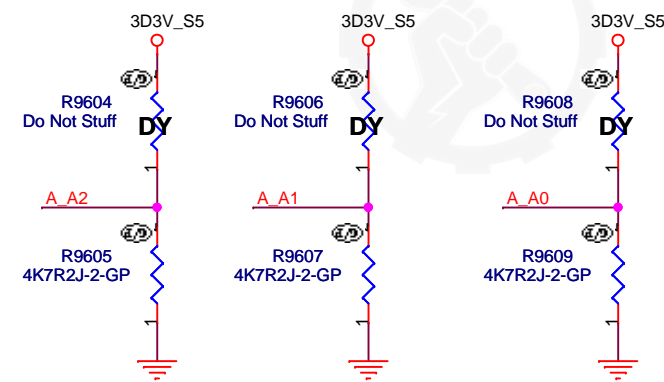


IT8010/IT8011/IT8012 difference

DEVICE	PIN8	PIN18
IT8010	NC	VSTBY33
IT8011	NC	VSTBY18
IT8012	VCOREI	VSTBY33

I2C SAD+Read/Write patterns

Command	SAD[7:4]	A[2]	A[1]	A[0]	R/W	SAD+R/W
Read	0100	0	0	0	1	01000001 (41h)
Write	0100	0	0	0	0	01000000 (40h)
Read	0100	0	0	1	1	01000011 (43h)
Write	0100	0	0	1	0	01000010 (42h)
Read	0100	1	1	1	1	01001111 (4Fh)
Write	0100	1	1	1	0	01001110 (4Eh)



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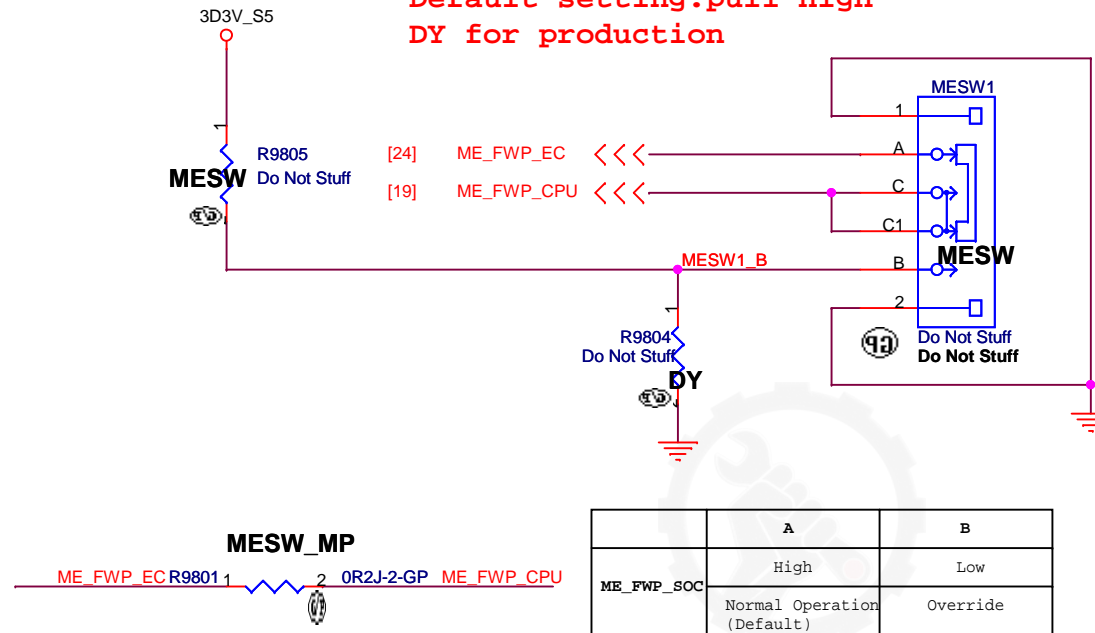
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Taos KBL-U

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LVDS Switch

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Default setting:pull high
DY for production

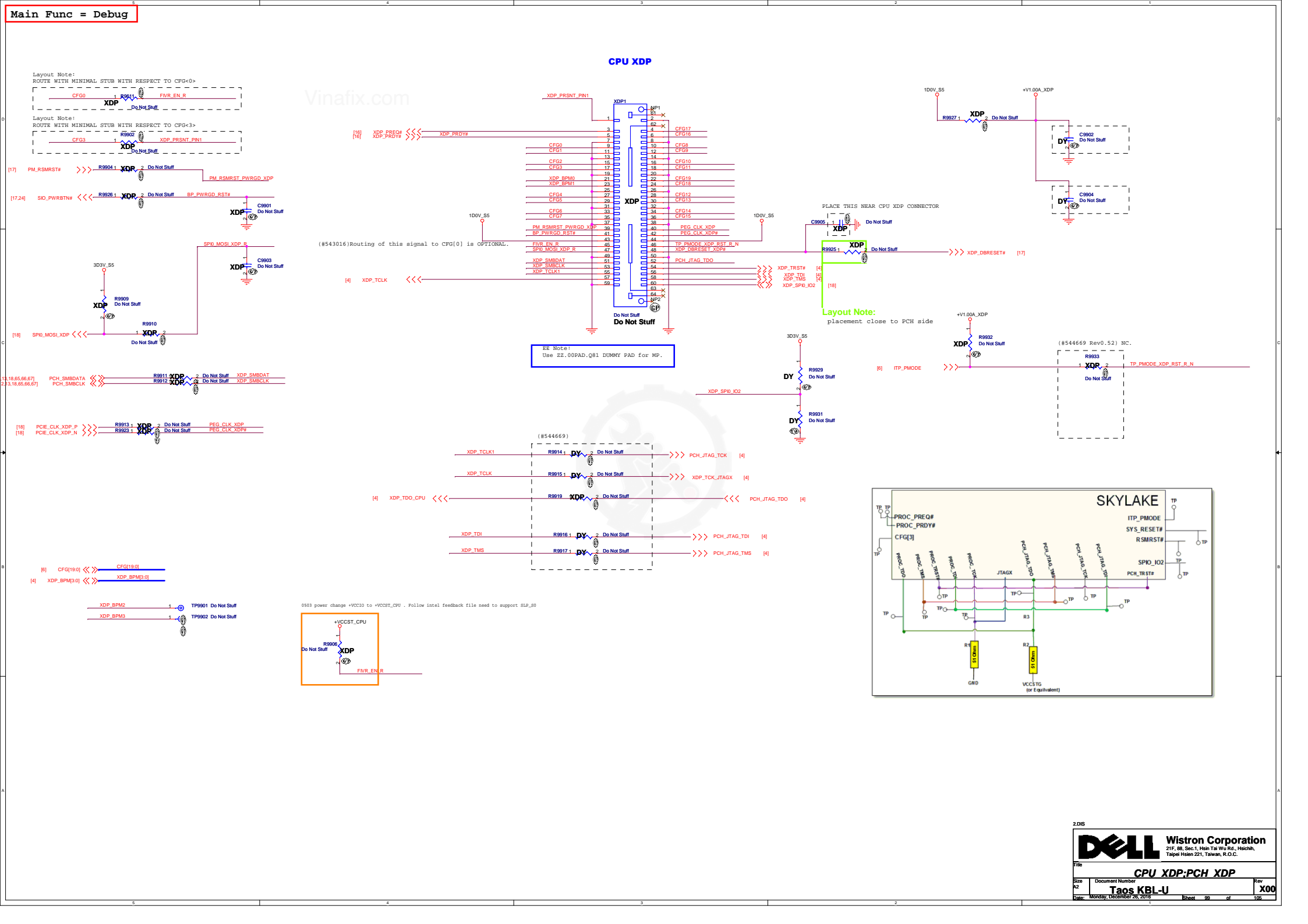


Firmware SW

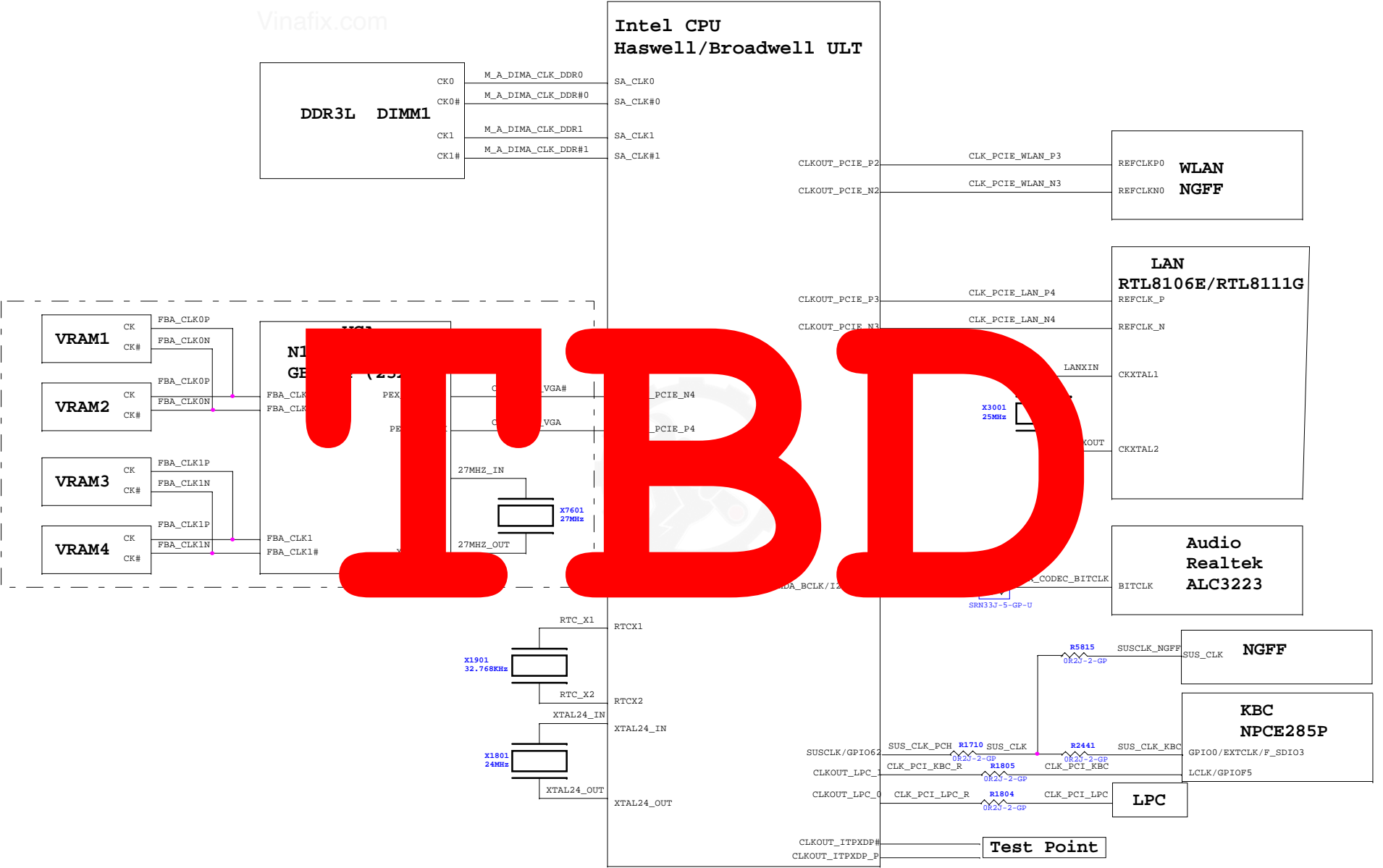
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CLK Block Diagram



Change notes -

[illegible]

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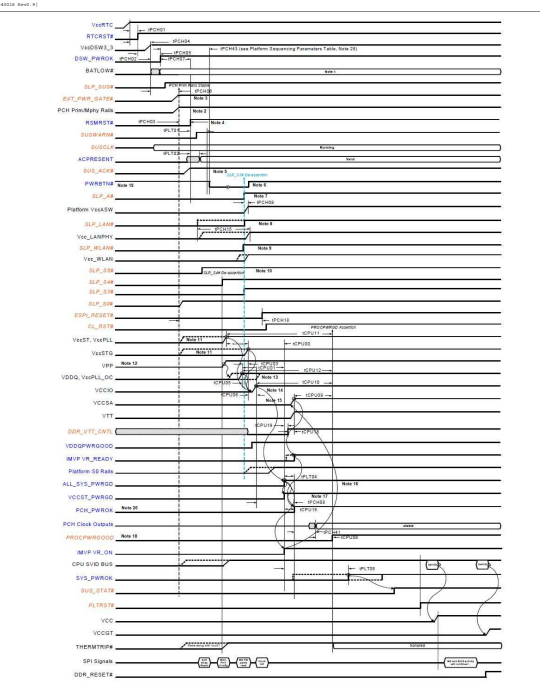
Rev

X00

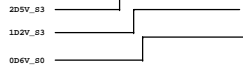
Date: Monday, December 26, 2016

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SKL-UYY Timing Diagram for G3 to S0/M30 [Deep Sx Platform]



For DDR4 power sequence



AMD GPU Power sequence

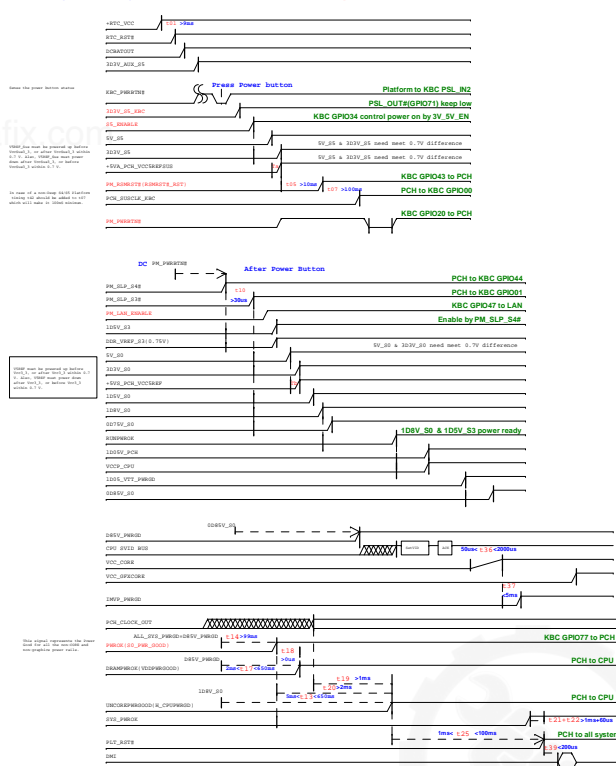
3DV_VGA0
=> 0.95V_VGA_0/1DV_VGA_0
=> 1DV_VGA_0
=> VGA_CORE

20ms

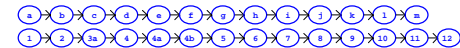
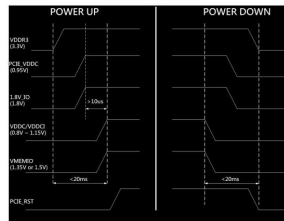
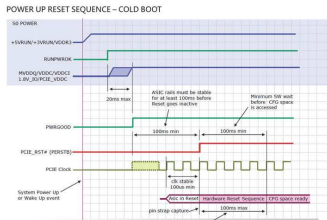
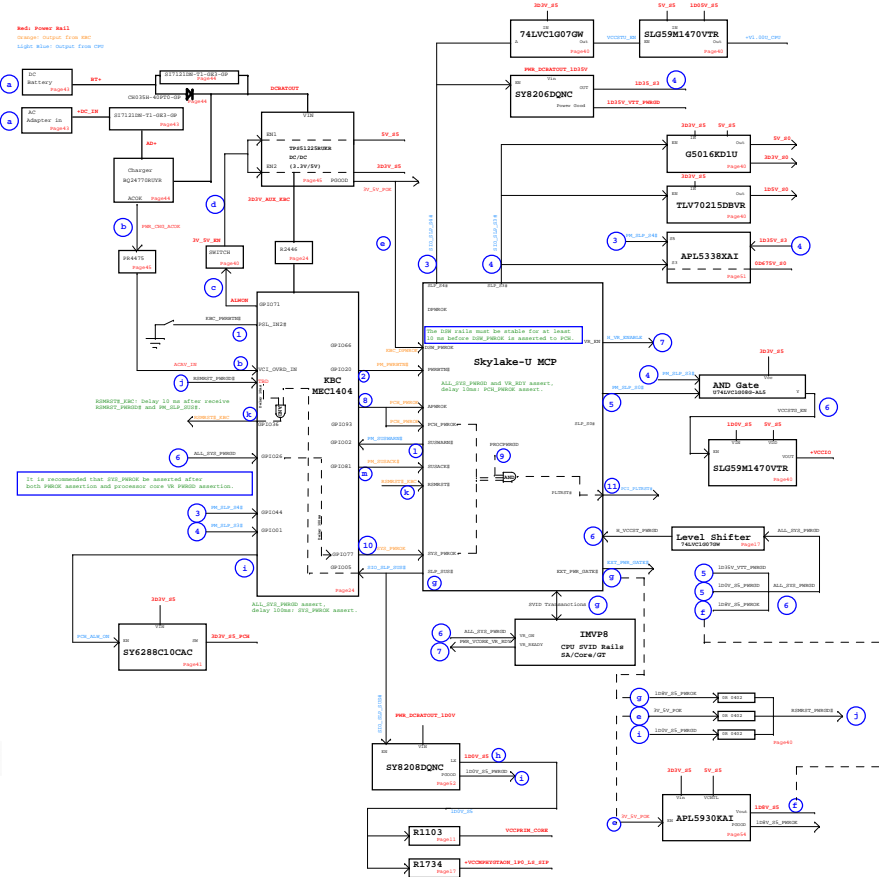
All the ASIC supplies must reach their respective nominal voltages within of the start of the ramp-up sequence, though a shorter ramp-up duration is preferred. The maximum slew rate on all rails is 50mV/us. It is recommended that the 0.95V rail ramp up first. It is recommended that the 0.95V rail reach at least 90% of its normal value no later than 2ms from the start of VDDQ ramping up.



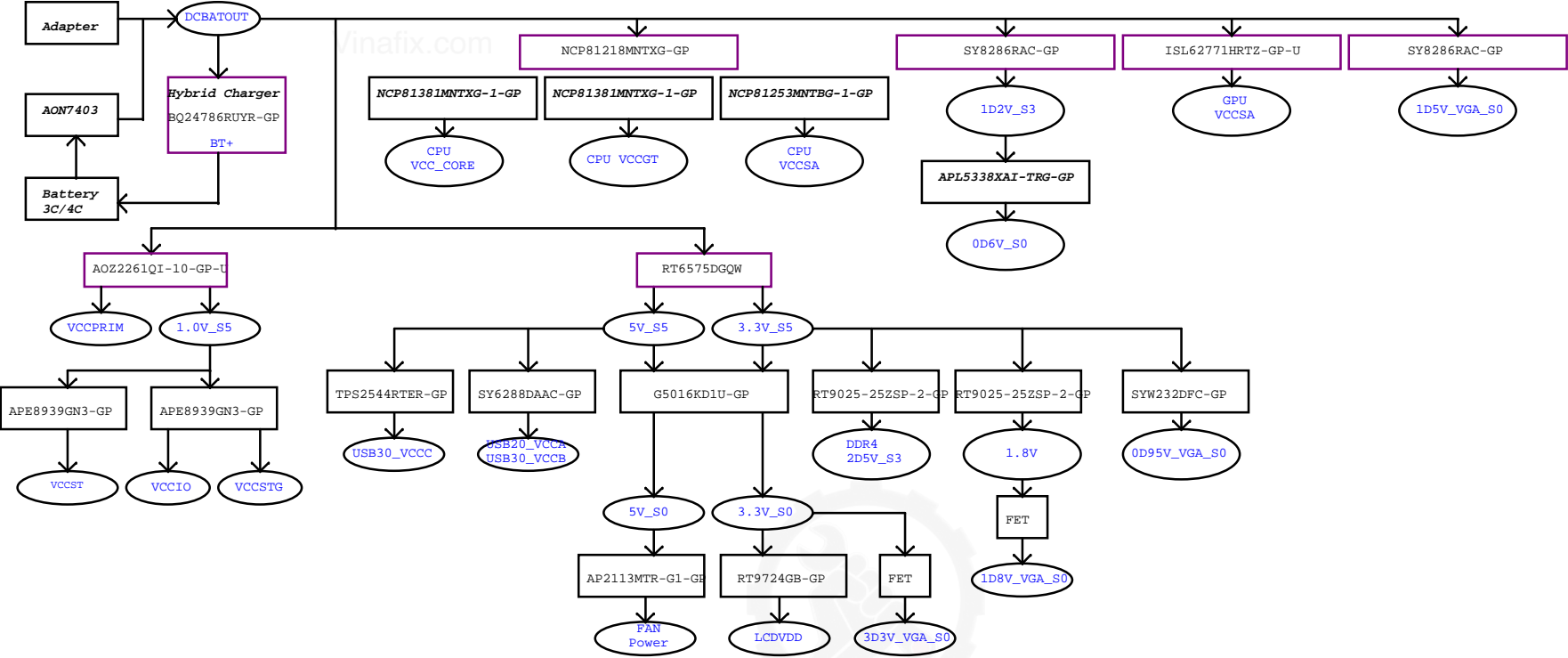
(DC mode)



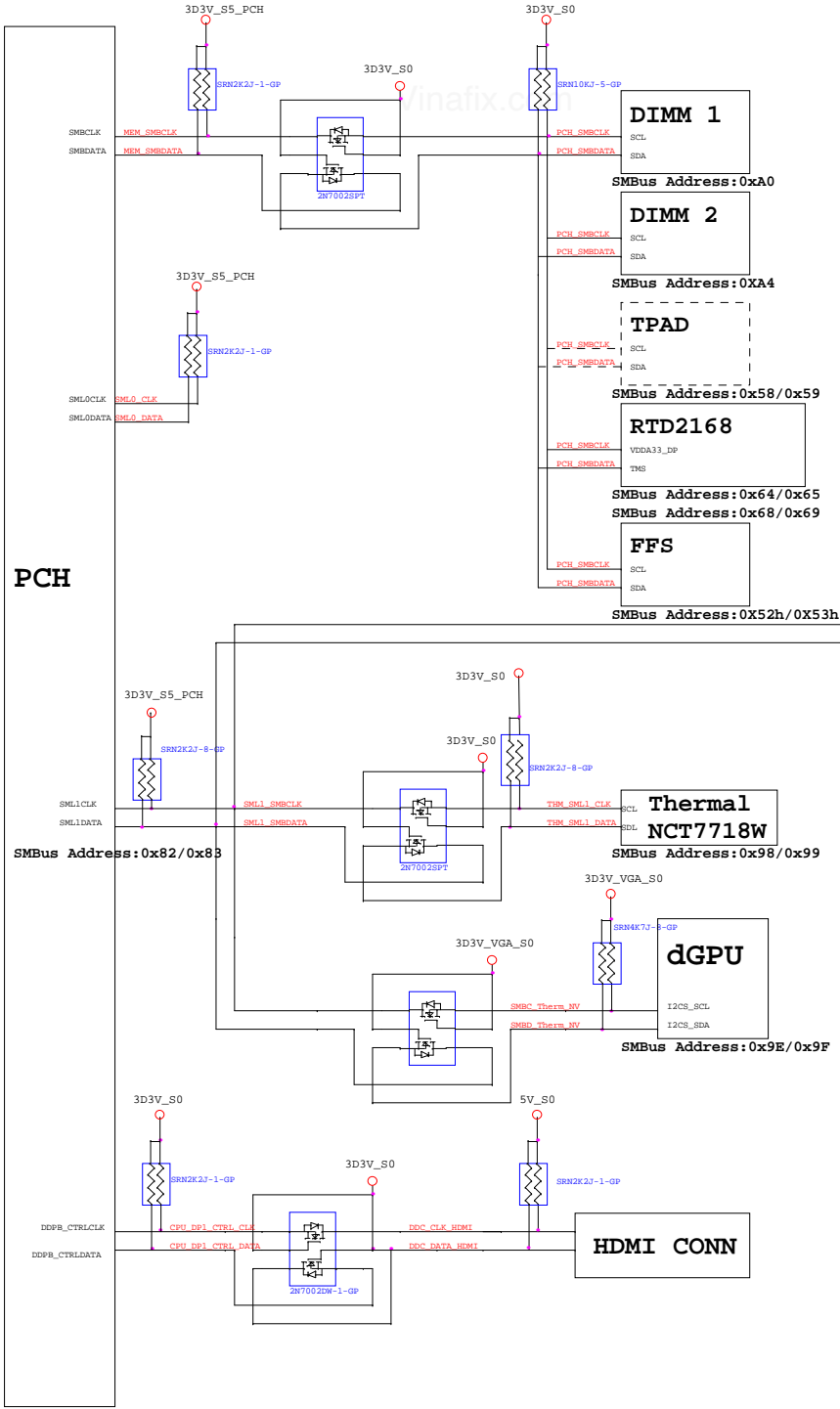
Taos Skylake POWER UP SEQUENCE DIAGRAM (Deep Sx Platform)



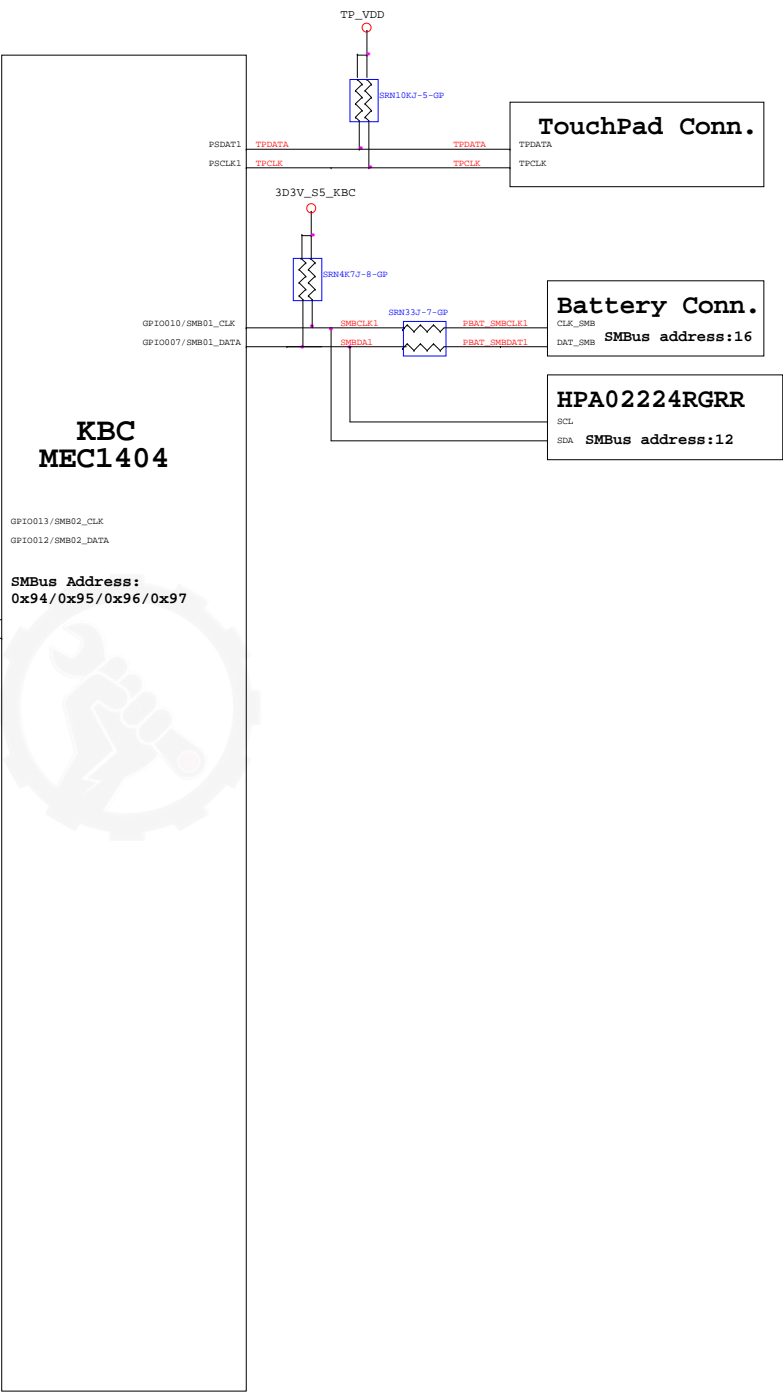
Taos Power Block Diagram



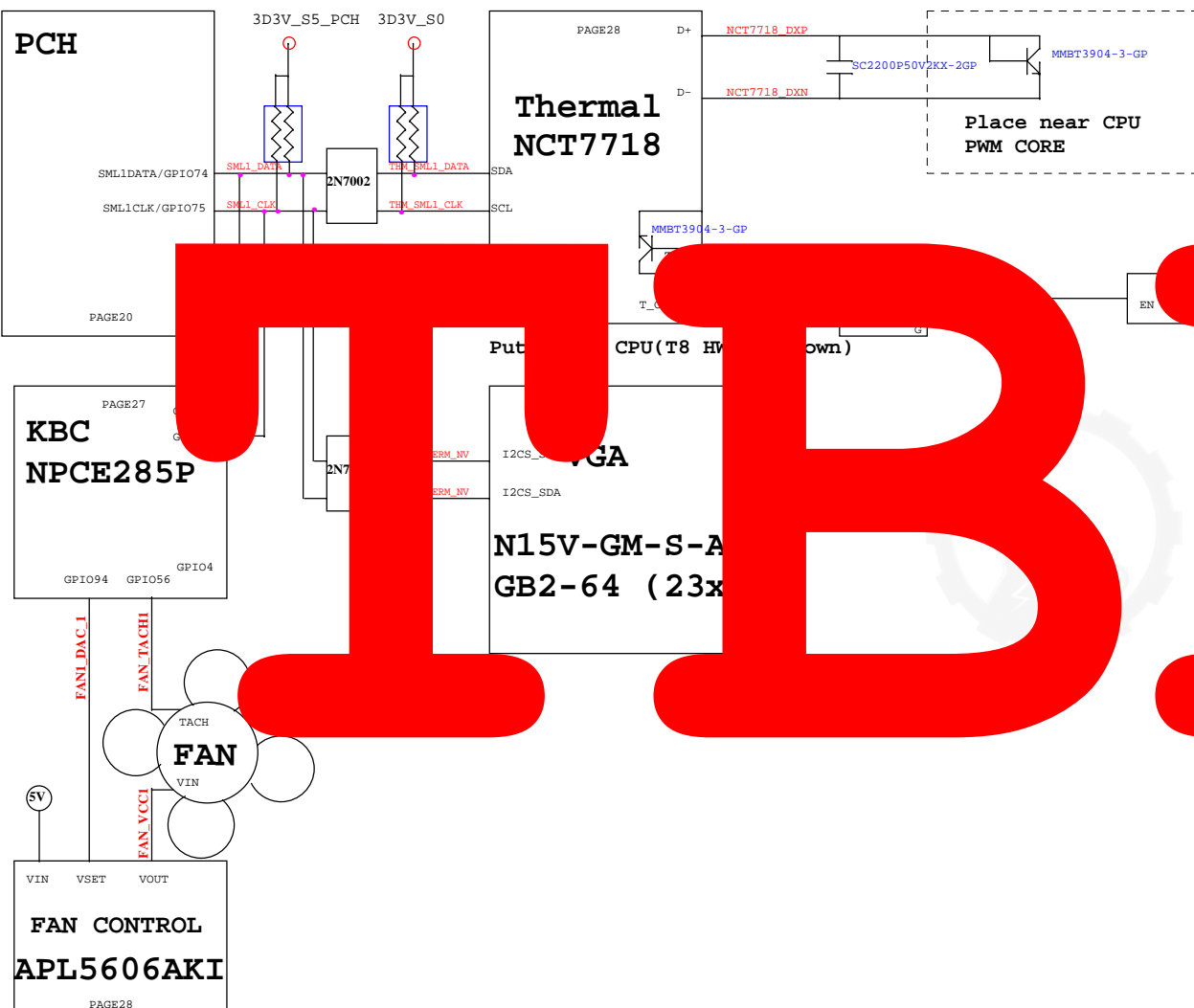
PCH SMBus Block Diagram



KBC SMBus Block Diagram



Thermal Block Diagram



Audio Block Diagram

